Colour television

Service
Service
Service

Anubis B

Circuit Description

Contents

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1. Introduction

Contents

The Anubis B chassis is a new chassis for small screen televisions with a screen size of 14", 15", 17" and 21". The circuits are situated on the mono-panel and in several separate modules. The mono-panel is of modular construction, which means that all functional components of a specific circuit are located within one module on the mono-panel. (see Fig. 1.1).

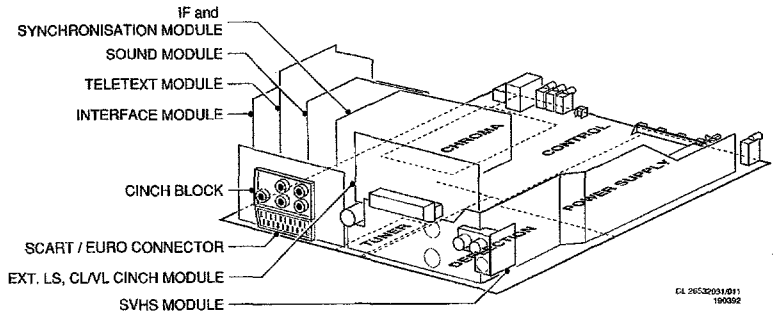


Fig. 1.1

This, together with the "Service Default Mode", "Error Messages" and the Test Points" make rapid diagnosis and therefore good service possible.

The Anubis B is equipped with menu operation; an installation menu for automatic tuning, system choice and the storage of various information and operating menus for picture, sound and various. The menus can be called up by means of the respective operating buttons (Fig. 1.2).

1.1 Repair provisions

Test points

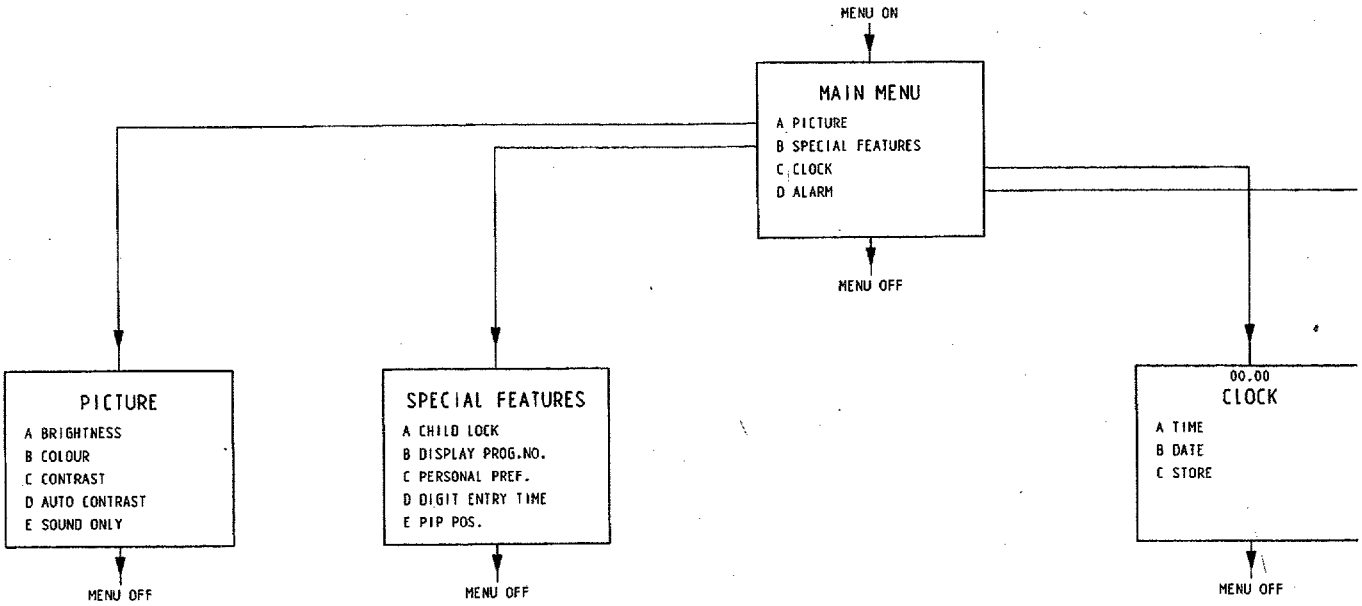
The Anubis B chassis is equipped with test points, TP1, TP2 etc. in the service printing on the component side of the mono-panel. With the aid of these test points it is possible to make a rapid diagnosis from the upper side of the mono-panel. These test points are also referenced in the service manual.

Service Default Mode

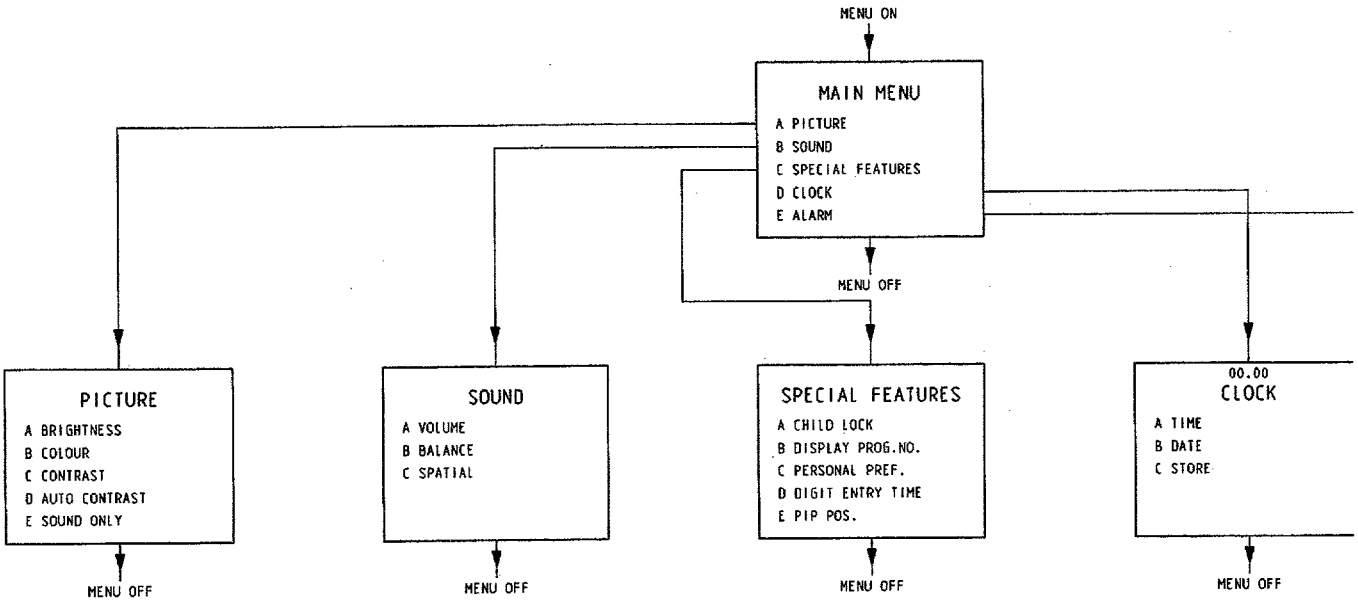
The software of the Anubis A also includes a so-called "Service Default Mode". To activate this mode it is necessary to connect service pins M61 and M62 on the carrier panel, and the set must be switched on using the mains switch.
To indicate that the set is in the Service Default Mode an "S" appears on the screen, followed by 5 numbers. The 5 numbers indicate the last 5 detected faults, which enables intermittent faults to be easily traced, last detected error on the left side.
In case the Service Default Mode is activated the set is placed in a pre-defined condition in which all functions are set in the intermediate position and the set is tuned to program 1. All DC voltages and oscillograms indicated in the service manual have been measured in this pre-defined condition.
The Service Default Mode can be exited by switching the set into stand-by using the remote control.

Operation menus

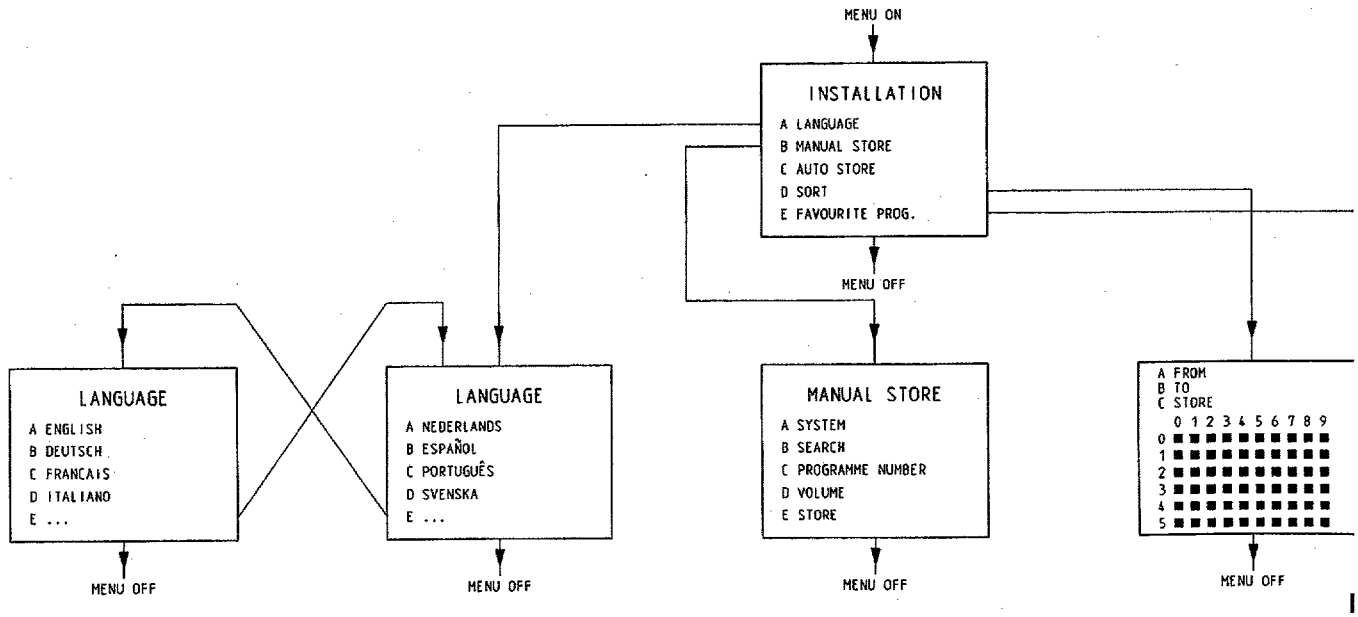
MONO



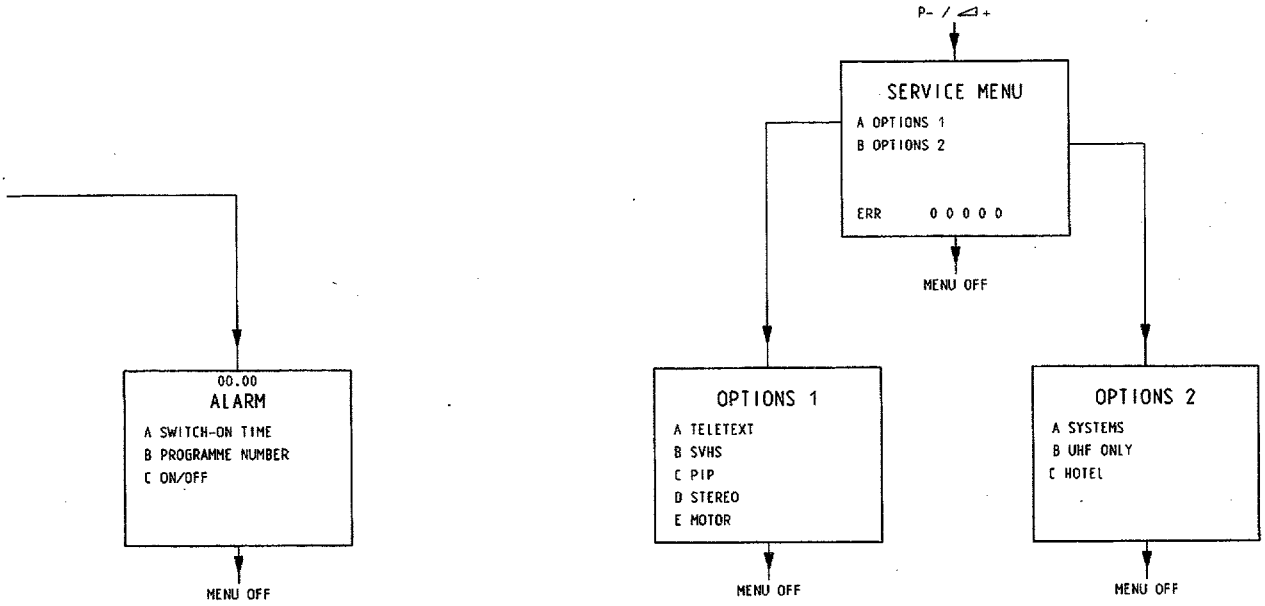
STEREO

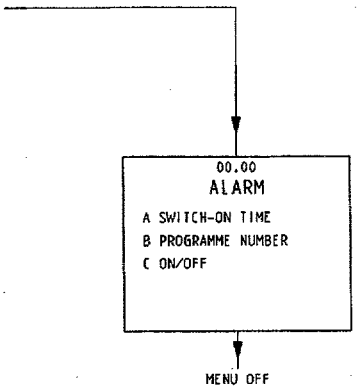


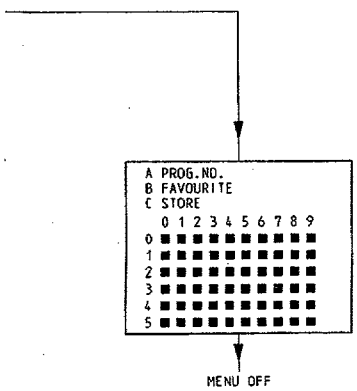
INSTALL



SERVICE DEFAULT MODE







CL26532032/046,G001
030492

Service Menu

By operating the "menu" key on the remote control when in the Service Default Mode (or by simultaneously pressing the volume+ and program buttons on the set) the set will enter service mode. In the service mode the options (SVHS, system etc.) can be selected. The software in the set is then capable of operating the selected functions.

Error messages

The microcomputer also has IC (Inter IC bus) software error detection which makes error messages from specific circuits visible via the OSD (On Screen Display) and a flashing LED.

1.2 The block diagram (Fig. 1.3)

With the Anubis B the circuits are located on the chassis and various plug-in panels.
Besides the functional division of the modules, the chassis is also divided up into functional blocks. The names of these functional blocks can also be found on the service printing on the panel.

Tuner

Channel selector
The channel selector is located at position 1901, a UV917 for VHF-UHF-S selection, a UV915 for VHF-UHF-S-Hyperband reception or a U943 for only UHF reception. The channel selector is tuned following the VST principle. Band switching is performed by IC 7010 (LA7910) and a three from two decoder.

IF/SYNC

MF/Synchronisation
IC 7300 (TDA4504) contains the video-intermediate frequency amplifier, intermediate frequency detector, video switchingand the synchronisation circuits. In mono FM sets the sound is also fed through this intermediate frequency.

Chrominance

The chrominance module is built up from IC 7250 (TDA465C a multi standard colour decoder, or IC7260 (TDA4510) a PAL colour decoder, IC 7290 (TDA4661) the base band delay line and IC 7280 (TDA3504), the video controller IC. The RGB output amplifiers are located on the picture tube panel.

Deflection

The horizontal output stage is formed by transistor 7445 anc the horizontal output transformer 5445. The horizontal output stage provides the high voltage and the focusing voltage, and also provides the +163V, +7, +13 and the +26 supply voltages.
IC 7400 (TDA3653) provides the vertical deflection.

AM/FM Stereo

For stereo FM or AM sound use is made of a second intermediate frequency amplifier in IC 7100 (TDA3843 for AM, TDA3845 for stereo FM & AM).

FM Sound

For the demodulation of FM modulated sound use is made of IC 7100 (TDA3827). Switching between AM, FM or Audio from the Euro-connector is also achieved with the aid of this IC.

In stereo sets IC 7140 is used for the demodulation of the second carrier wave. IC 7806 is used for switching between mono and stereo, and between language I and language II. This choice has to be made by the user personally. A detection circuit indicates whether a second carrier wave is being received.

IC 7130 (mono/right) and IC 7160 (left) have been included as sound amplifiers.

Power supply

The mains isolated power supply is formed by mosfet transistor 7525 and transformer 5525 and is of the Self Oscillating Power Supply (S.O.P.S.) type.
The power supply provides the +95, +12 and +5 supply voltages.

Controls

Control is accomplished by the microcomputer IC 7600(P83C054BBPNB).

Euro

The Anubis B is equipped with a Euro (scart) connector and an SVHS connector. The source choice for the picture takes place in IC 7805 (CD4052), the source choice for sound in IC 7807 (CD4052) and if PIP is available, PIP source choice in IC 7806 (CD4052). The SVHS signals are then first mixed into a CVBS signal.

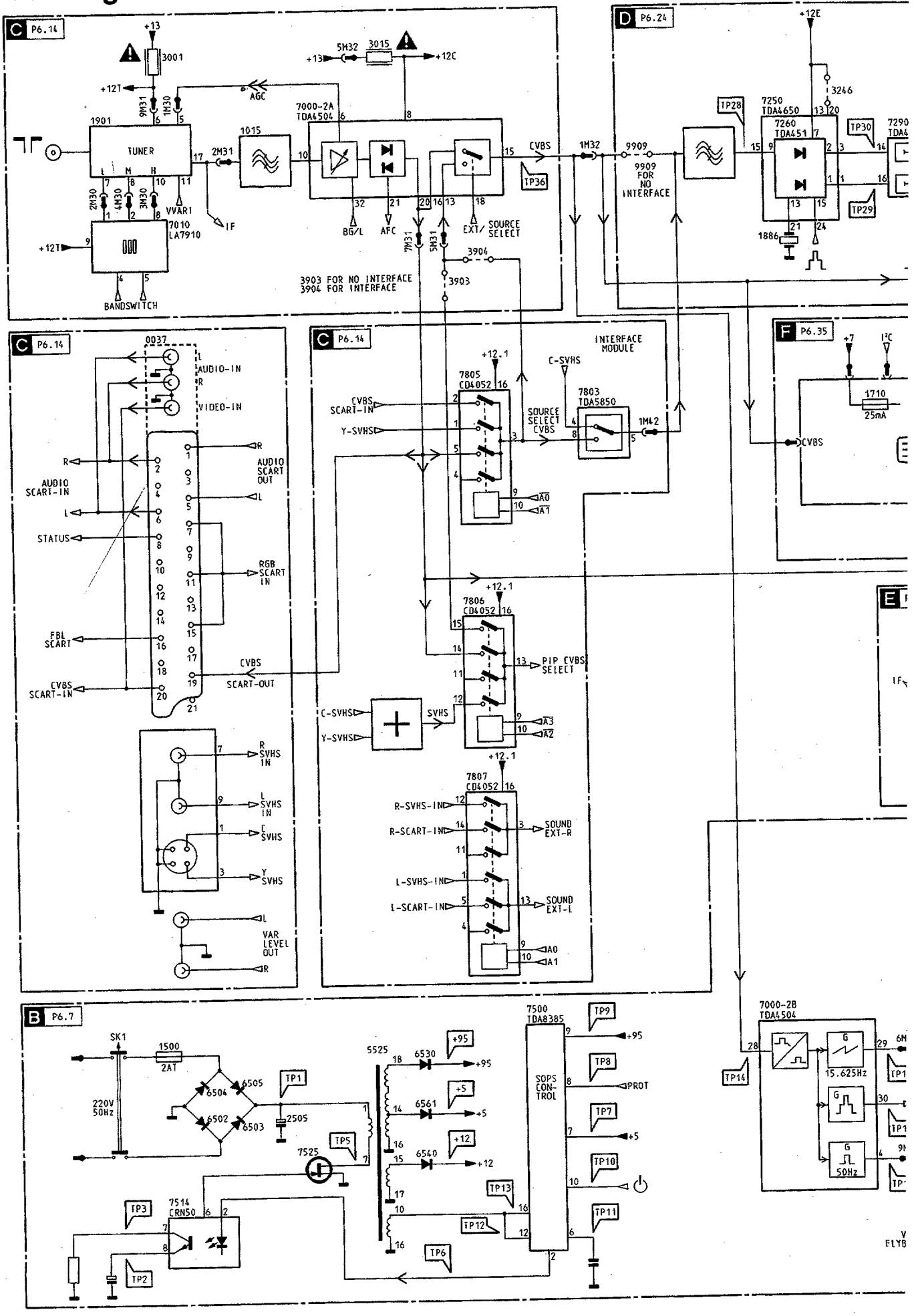
TXT

The Anubis B can be equipped with a CCT (Computer Controlled Teletext) teletext decoder. The RGB teletext information is sent to video controller IC 7280 (TDA3504).

Picture in Picture

The picture in picture RGB information from the PIP module is multiplexed on the PIP module with the RGB information from the Euro connector. The RGB information is subsequently mixed with the TXT information and sent to the video controller (IC 7280/TDA3504).

Blockdiagram / Blockschaltbild / Schéma-bloc



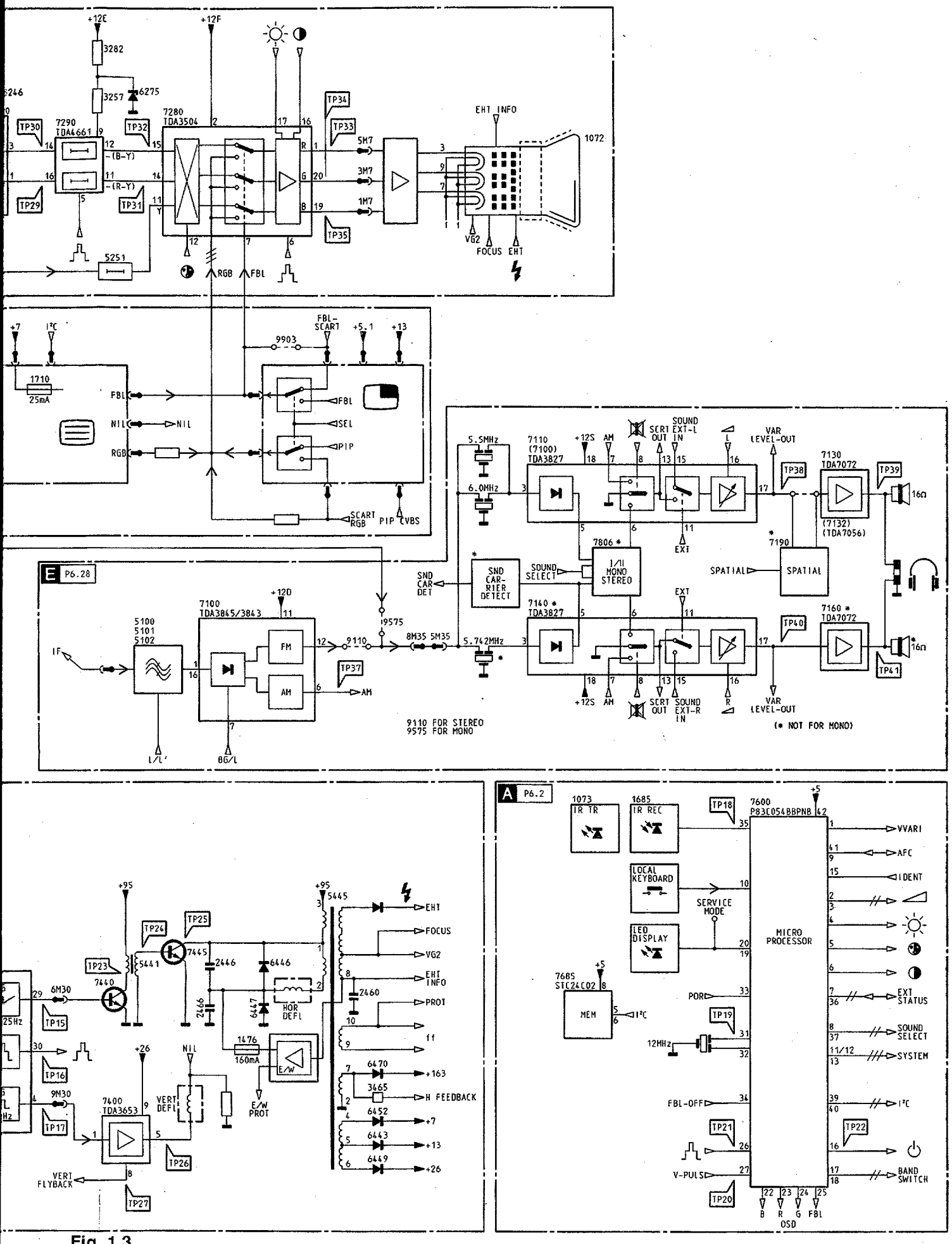

+12E
+12F
3282
3257
6275
TP30
TP32
7290
TDA4661
7280
TDA3504
TP34
TP33
EHT INFO
1072
5M7
3M7
1M7
-(B-Y)
-(R-Y)
TP29
TP31
TP35
5251
VG2
FOCUS
EHT
RGB
FBL
FBL-
SCART
+5.1
+13
9903
+7
I²C
1710
25mA
NIL
SEL
PIP
SCART
RGB
PIP
CVBS
E P6.28
5.5MHz
6.0MHz
7110
(7100)
TDA3827
+12S
AM
SCRT
OUT
SOUND
EXT-L
IN
VAR
LEVEL-OUT
7130
TDA7072
TP38
TP39
16Ω
(7132)
(TDA7056)
EXT
7806 *
7190
SND
CAR-
RIER
DETECT
SOUND
SELECT
I/II
MONO
STEREO
SPATIAL
SPATIAL
7100
TDA3845/3843
+12D
5100
5101
5102
IF
FM
AM
TP37
9110
9575
8M35
5M35
5.742MHz
7140 *
TDA3827
TP40
7160 *
TDA7072
TP41
SCRT
OUT
SOUND
EXT-R
IN
VAR
LEVEL-OUT
9110 FOR STEREO
9575 FOR MONO
(* NOT FOR MONO)
L/L'
BG/L
+95
5445
TP24
TP25
TP23
7445
7440
5441
2446
6446
2466
6447
HOR
DEFL
6M30
TP15
25Hz
30
TP16
9M30
TP17
+26
NIL
1476
160mA
E/W
E/W
PROT
VERT
DEFL
7400
TDA3653
TP26
VERT
FLYBACK
TP27
EHT
FOCUS
VG2
EHT
INFO
PROT
2460
11
6470
+163
3465
H FEEDBACK
6452
+7
6443
+13
6449
+26
A P6.2
1073
IR TR
1685
IR REC
TP18
7600
P83C054BBPNB
+5
LOCAL
KEYBOARD
SERVICE
MODE
LED
DISPLAY
MICRO
PROCESSOR
7685
ST24C02
MEM
I²C
POR
TP19
12MHz
FBL-OFF
TP21
V-PULS
TP20
TP22
VVARI
AFC
IDENT
EXT
STATUS
SOUND
SELECT
SYSTEM
I²C
BAND
SWITCH
B
R
G
FBL
OSD

Fig. 1.3

2. Operation

All operation and control functions are built around a 42 pin microcomputer IC 7600 of the type P83C054 (Fig. 2.1).

Power-on reset (POR)

The (12MHz) microcomputer oscillator frequency is made available on pins 31 and 32 with the aid of the crystal. In order to allow the microcomputer to start correctly a POR (Power On Reset) pulse is given on pin 33 when the set is switched on via the mains switch. Initialisation then takes places and the microcomputer starts up.

Keyboard

There are 5 keys located on the keyboard (Volume+/-, Program +/- and Installation). Each switch is connected to +5 volt. When a key is operated the +5 volt is fed to a voltage distribution unit that consists of a resistor belonging to the key (3640, 3642, 3643, 3644 and 3646) and the common resistor R3645. The distributed voltage is fed to pin 10 of IC 7600. As each switch operates a different resistor, a different voltage is available on pin 10, enabling the microcomputer to detect which key has been operated.

System switching voltages

The switching voltages are available for BG/L, L/L' and I on pins 11, 12 and 13 respectively. Transistors TS7654, TS7672 and TS7674 invert the switching signals and operate the intermediate frequencies IC's for audio and video.

On screen display

With the aid of the OSD generator information is displayed on the screen concerning the tuned band, the location in the tuning area, selected system, sleep timer, program number and the positions of the various picture and sound adjustment controls.
The OSD information is provided by the R, G and B signals on pins 22, 24 and 23. The permanent fast blanking signal is available on pin 25.
The OSD information is synchronised with the main picture by the sandcastle pulse. Transistor TS7670 keys the burstkey from the sandcastle and feeds this through to pin 26/IC 7600. Transistor TS7665 keys the vertical synchronisation pulse from the sandcastle, following buffering by TS7660, and feeds this through to pin 27/IC 7600.
The OSD generator is controlled by its own oscillator with oscillator circuit C2677, C2678 and L5677.

Memory

The microcomputer is connected via the I^2C bus to a non-volatile memory IC7685 (EAROM). The preference and program information is stored in this memory.

Picture and sound controls

There are 5 analogue adjustments, namely; volume 1 (pin 3), volume 2 (pin 2), brightness (pin 4), colour saturation (pin 5) and contrast (pin 6). Volume 1 controls volume for the right channel and volume 2 the left channel. Adjusting the relationship between the two volume channels enables the balance to be adjusted.
The adjustment outputs of IC 7600 are pulse-width modulated. With the aid of RC networks the pulse width modulated signals are converted to DC current. Sound suppression takes place internally in the microcomputer by lowering the volume.

Auto contrast

Transistor TS7613 is the sensor for the auto contrast circuit. When switched in, the microcomputer (IC 7600) sets contrast (pin 6) at maximum. The circuit is switched in via pin 38/IC 7600, following which the contrast adjusting signal is modified by the amount of incidental light via TS7601 and TS7612.

Tuning

The tuning system is based on VST (Voltage Synthesized Tuning). This system is based on the principle that tuning to a transmitter in the set is obtained by a linear variation of the tuning voltage (Vvari).The tuning voltage (0V2 to 5V) is available on pin 1 of the microcomputer and taken to the correct level by the +95. The AFC (Automatic Frequency Control) that is added to the tuning voltage is switched out during transmitter searches by pin 41. If an IDENT signal is received on pin 15 during transmitter searches, the microcomputer makes a check on correct tuning via pin 9 to see whether the AFC can be switched back in.
To enable band switching the microprocessor has two band switching voltages on pins 17 and 18.

Stand-by

The stand-by NOT switching signal is available on pin 16 of the microcomputer. This enables the microcomputer to switch the power supply into stand-by.
The LED on pin 20 illuminates red on stand-by, is green during normal operation and orange when receiving RC5 commands.

Sound selection

A signal is fed to pin 14 which indicates whether a second sound carrier wave is being received. In that case LED 6613 will illuminate. This signal does not indicate whether a stereo or a bilingual broadcast is being received. The user must personally select language I, language II or stereo. Mono sound is always selected as standard. The voltage on the sound select output (pin 8/IC 7600) is used to select stereo, mono, language I or language II.

Spatial

In stereo sets pin 37/IC 7600 can be used to switch in the spatial stereo effect.

Status external in

If a status voltage is offered on pin 8 of the Euro connector pin 36/IC 7600 goes low. The microcomputer now selects the sound and picture signals on the external input via pin 7/ IC 7600.
If, in addition to the status voltage on pin 8 of the Euro connector, a fast blanking signal is offered on pin 16, the RGB signal being offered will be selected. If the TV mode is now selected the fast blanking signal from the Euro connector will be suppressed via pin 34/ IC 7600, which will result in the reselection of the signal from the tuner.

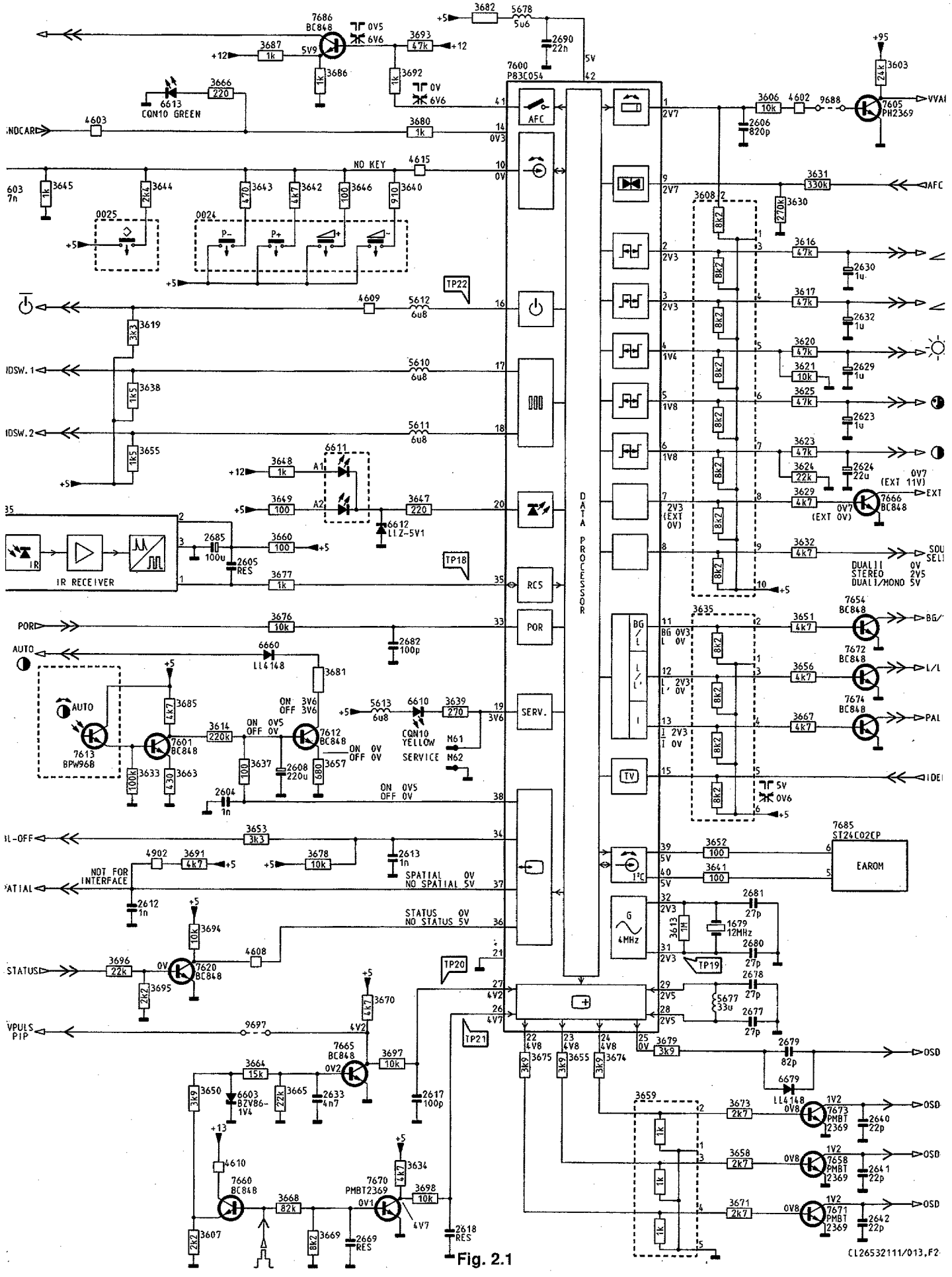

7600
P83C054
DATA PROCESSOR
AFC
RCS
POR
SERV.
TP18
TP19
TP20
TP21
TP22
IR RECEIVER
6613
CQM10 GREEN
6612
LLIZ-5V1
CQM10
YELLOW
SERVICE
M61
M62
7613
BPW96B
7601
BC848
7612
BC848
7620
BC848
7660
BC848
7665
BC848
7670
PMBT2369
7671
PMBT
2369
7672
BC848
7673
PMBT
2369
7674
BC848
7654
BC848
7658
PMBT
2369
7666
BC848
7605
PH2369
6660
LL4148
6679
LL4148
6603
BZV86-
1V4
7685
ST24C02CP
EAROM
4MHz
12MHz
NOT FOR
INTERFACE
SPATIAL 0V
NO SPATIAL 5V
STATUS 0V
NO STATUS 5V
DUALII 0V
STEREO 2V5
DUALI/MONO 5V
0V7
(EXT 11V)
0V7
(EXT 0V)
2V3
(EXT
0V)
ON 3V6
OFF 3V6
ON 0V5
OFF 0V
ON 0V
OFF 0V
ON 0V5
OFF 0V
NO KEY
0025
0024
P-
P+
IDSW.1
IDSW.2
INDCARL
PURS
PIP
STATUS
SPATIAL
AUTO
POR
OSD
EXT
AFC
VVAI
IDEI
SOU
SELI
BG/
L/L
PAL

Fig. 2.1

Contents

3. Channel selector and intermediate frequency

3.1 Channel selector

The channel selector 1901 (see Fig. 3.1) is a UV917, UV915 or a U943. The U943 is a channel selector which is only suitable for reception in the high band. (see table 1).
The UV917 is suitable for reception in the low band, the mid band and the high band, the UV915 is also suitable for the reception of the hyper band. In the case of a UV915 and UV917 channel selector, IC 7775 (LA7910) - a three from two decoder - controls band switching via pins 7, 8 and 10 on the channel selector.

Low band: 46 - 118 MHz (VHFI + S)
Mid band: 118 - 350 MHz (S + VHFIII) UV917
Mid band: 118 - 450 MHz (S + VHFIII + Hyper) UV915
High band: 450 - 861 MHz (UHF)

	BAND	IC7010 3 4	1901 7 8 9
U943	HIGH	NOT PRESENT	L L H
UV917	LOW	L L	H L L
UV915	MID	H L	L H L
	HIGH	H H	L L H

Table 1

The tuning voltage V_{vari} is supplied via pin 11 and the AGC (Automatic Gain Control) voltage via pin 5.
The 38.9 MHz intermediate frequency signal is available on the channel selector output pin 17 (33,4 MHz if a SECAM L' signal is offered).

3.2 Intermediate frequency filter

The intermediate frequency filter characteristic is determined by band filter 1301.
For PAL/SECAM BG sets only a 5.5 MHz SAW (Surface Acoustic Wave) filter is used.
On reception of L'/I systems (switching signal BG/L "high") no modification takes place and the filter band width is 6 MHz.
On reception of BGL systems the switching signal BG/L is "low". This causes the band-stop filter L5305/C2326 to switch parallel on the filter input, causing the band width to bereturned to 5.5 MHz.
For sets that can only receive the PAL I system a filter with a band width of 6.0 MHz is used for 1301.

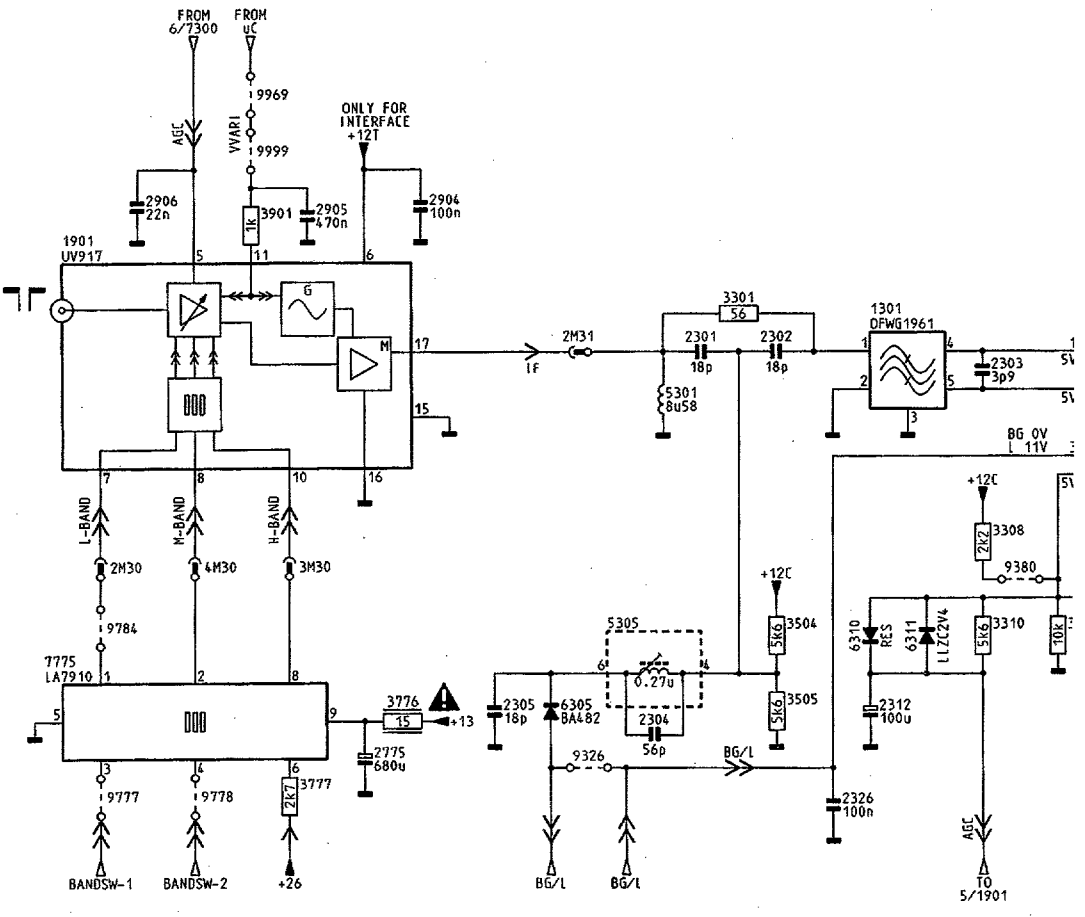
Demodulation AGC

The intermediate frequency signal is fed to IC 7300 pins 9 and 10. This IC is suitable for both negative (BG) and positive (LL') modulation depending on the switching signal on pin 32/IC 7300.
At the same time the switching signal on pin 32 determines whether the AGC circuit adjusts the top-white level (positive modulation) or the top-sync level (negative modulation). The high frequency AGC voltage is available on pin 6.
The take-over level of the high frequency (delayed) AGC adjustment on pin 2 can be regulated by 3314.

The demodulation reference circuit 5320 on pins 23 and 24 (IC 7300) is adjusted to 38.9 MHz.

In connection with another intermediate frequency in the SECAM'L system (33.4 MHz) the demodulation reference circuit 5320 on pins 23 and 24 must be switchable. This is achieved by using the L/L' switching signal. If this signal is "high", then coil L5043 is switched parallel to L5040 and the circuit is tuned to 33.4 MHz.

The base band CVBS signal is available on pin 20 with a nominal amplitude of 2V. In case of an "FM (intercarrier) sound" this signal will also contain the 5.5 MHz sound signal. The sound signal is filtered with a 5.5 MHz (6.0 MHz PAL I) ceramic filter (1345/1346).



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Automatic Frequency Control AFC

The AFC signal on pin 21 is taken from the reference signal and adjustment for positive or negative modulation is made internally in the IC.

Source choice selection

The CVBS signal is fed back to the source selection switch in the IC via pin 16. With the aid of the status-switching signal on pin 18 a choice can be made between internal CVBS or a CVBS signal from an Euro connector.
The selected CVBS signal is then available on pin 15.

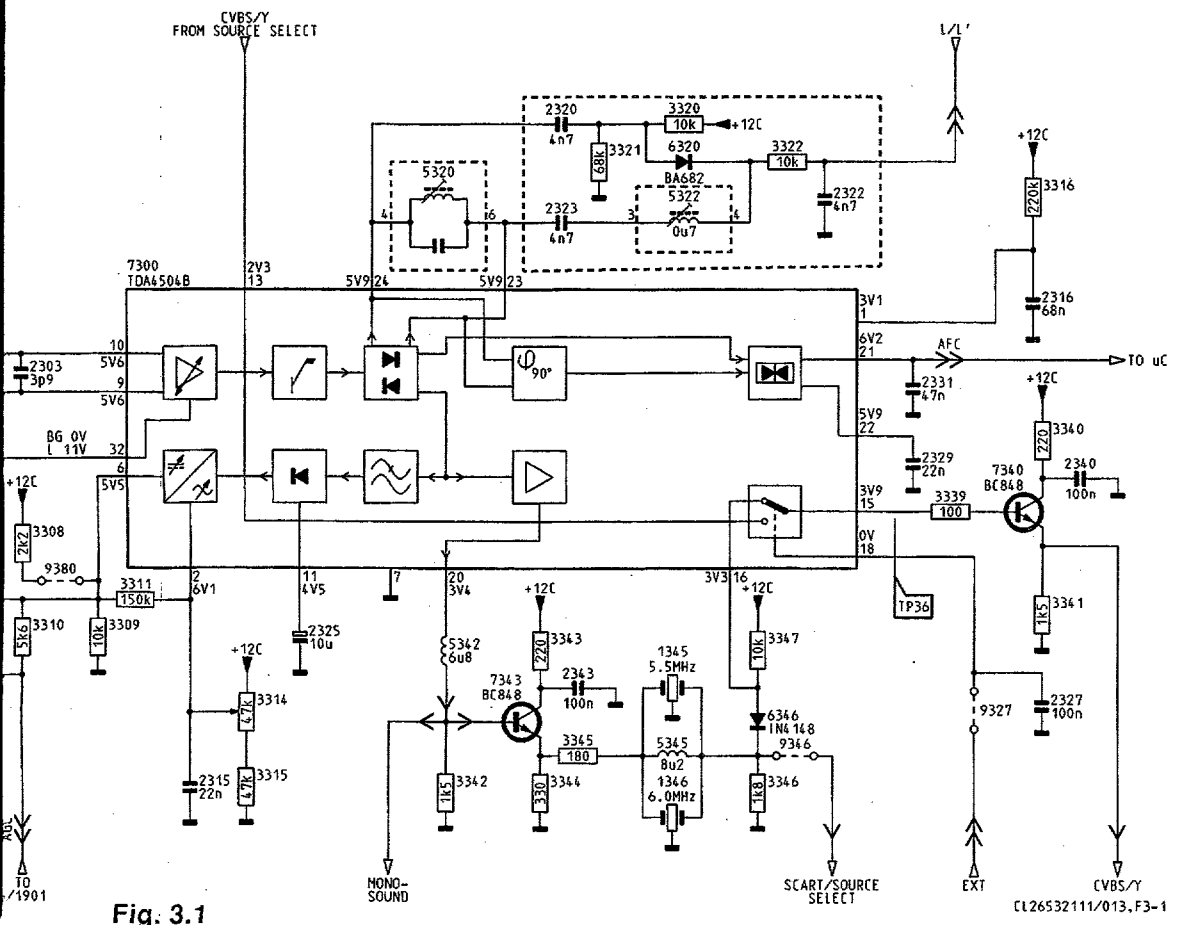


Fig. 3.1

4. Sound system

Contents

Two sound systems can be distinguished: for sets with only FM-mono reception the signal is taken from pin 20 on the video intermediate frequency (IC 7300). This signal is then taken to the sound modulator (IC 7100) via TS7576. For sets with stereo FM and/or AM, a separate sound intermediate frequency circuit has been added, built around IC 7593.

4.1 Sound MF (Fig. 4.1)

Filter 2578/5578 ensures that any 30.9 MHz interference signals are removed from the intermediate frequency signal from the channel selector. The signal is fed to input circuit 5587 of the intermediate frequency/AM demodulation IC 7593 (TDA3843 for AM, TDA3845 for stereo FM & AM) through filter 5584 which is equipped with a switchable filter characteristic. The switchable filter characteristic is necessary because the sound systems for PAL/SECAM BG, SECAM L and SECAM L' are all different. For AM sound signals (TDA3845) demodulation takes place with the aid of circuit 5593.
Switching systems is achieved with the switching signals BG/L and L/L'.

System BG

In the BG system both switching signals are low; Diodes 65 and 6585 do not conduct, diodes 6579, 6581, 6589 and 6582 conduct. Capacitors 2579, 2581, 2590 and 2106 also determine the filter's tuning.

System L

In the L system the switching signal BG/L is low; all switchir diodes conduct. Besides capacitors 2579, 2581, 2590 and 2106, capacitors 2587 and 2585 also determine the filter's tuning.

System L'

In system L' both switching signals are high; Diodes 6579, 6581, 6589 and 6582 do not conduct, diodes 6584 and 6585 conduct. Capacitors 2587 and 2585 now also determine the filter's tuning.
The modulated AM signal is available on pin 6 of IC 7593. The FM intermediate frequency signal is available on pin 12 of IC 7593.

4.2 Sound modules

Anubis B sets can be equipped with two different sound modules; a mono or a stereo sound module.

Mono sound module

The circuit of the mono sound module is identical to the mono channel of the stereo sound module. Specific functions such as sound choice, sound system choice and spatial are however not available on the mono sound module.

Stereo sound module (Fig. 4.2)

The stereo sound module consists of two independent channels. The volume of both channels can also be individually adjusted, also enabling balance adjustment in this manner. No detection system for the type of broadcast, i.e. stereo or bilingual, is available. A detection system does however indicate that a second carrier wave is being received. The user must then make a personal choice for mono, stereo or bilingual sound.

Mono/right/language I

For mono-FM modulated sound the mono sound signal is filtered out of the intermediate frequency signal by filter 1101 or 1102. Only in the case of PAL I being selected will the PAL I switching signal be low, 1102 will be parallel to 1101, and the filter tuning will be 6.0 MHz. At the same time this switching signal ensures that the demodulation circuit 5107/2109 of IC 7100 is tuned to 6.0 MHz and capacitors 2107 and 2108 are switched parallel to the filter.

Sound system choice

The modulated sound, pin 5, after de-emphasis and buffer switching around IC 7182, goes to selector IC 7185. The selected sound signal (pin 13) returns to pin 6 of IC 7110. The eventual AM modulated sound is available on pin 7 and using the voltage level on pin 8 a choice can be made between MUTE, or FM or AM sound.

Source selection and volume adjustment

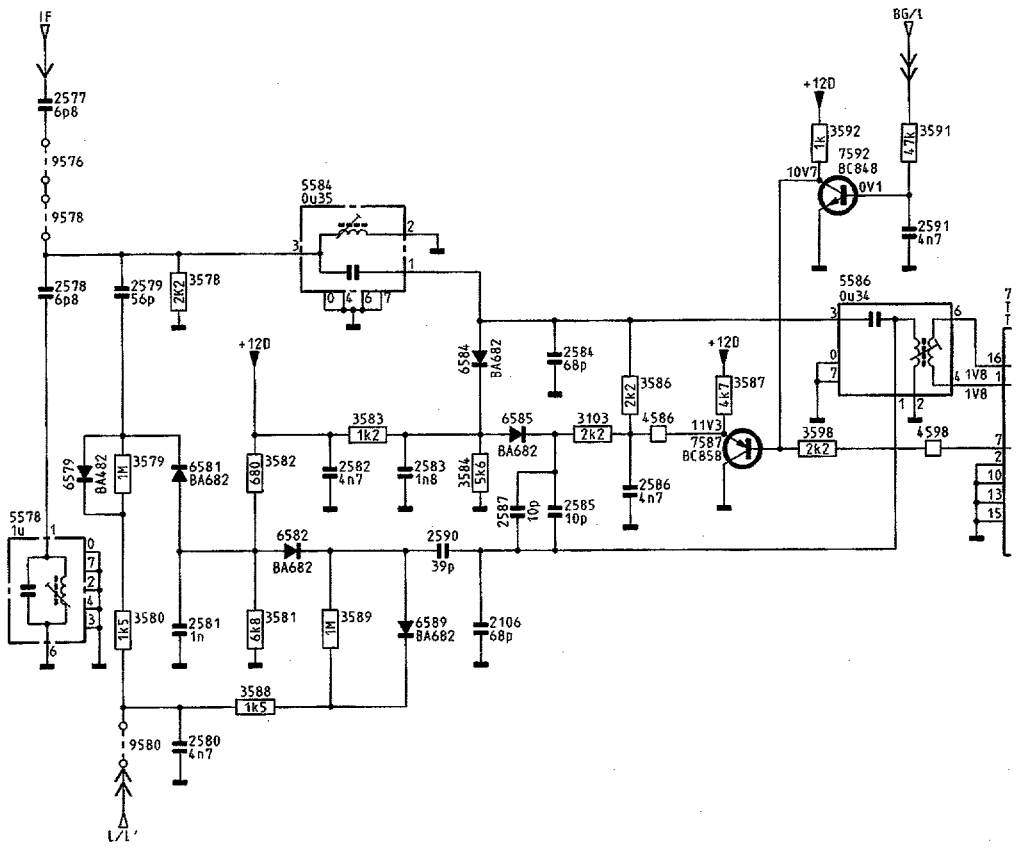
Following a choice for sound from the Euro connector (pin 11) or TV reception, the signal is fed via an amplifier and a source selection switch to an adjustable amplifier where the volume can be adjusted using the voltage on pin 16. The output signal on pin 17 is shorted to earth by TS7102 when the set is switched on in order to avoid switching sounds.

Left/language II

The sound signal from the second carrier wave (5.74 MHz) is filtered out of the intermediate frequency signal by filter 1140. The demodulation circuit 5143/2143 of IC 7140 is tuned to 5.74 MHz.

Sound system choice

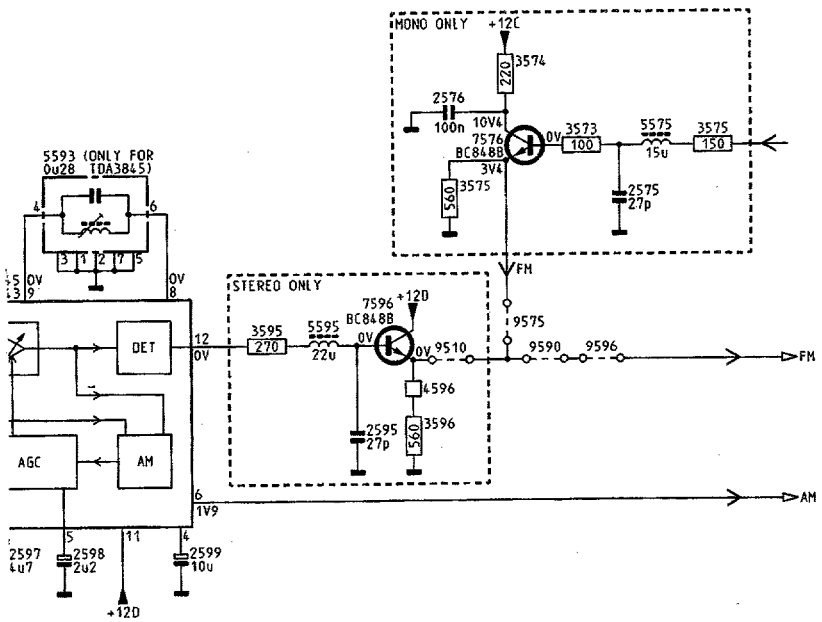
The modulated sound, pin 5, after de-emphasis and buffer switching around IC 7182 goes to selector IC 7185. The selected sound signal (pin 3) returns to pin 6 of IC 7140. The eventual AM modulated sound is available on pin 7 and usingthe voltage level on pin 8 a choice can be made between MUTE, or FM or AM sound.



Fig

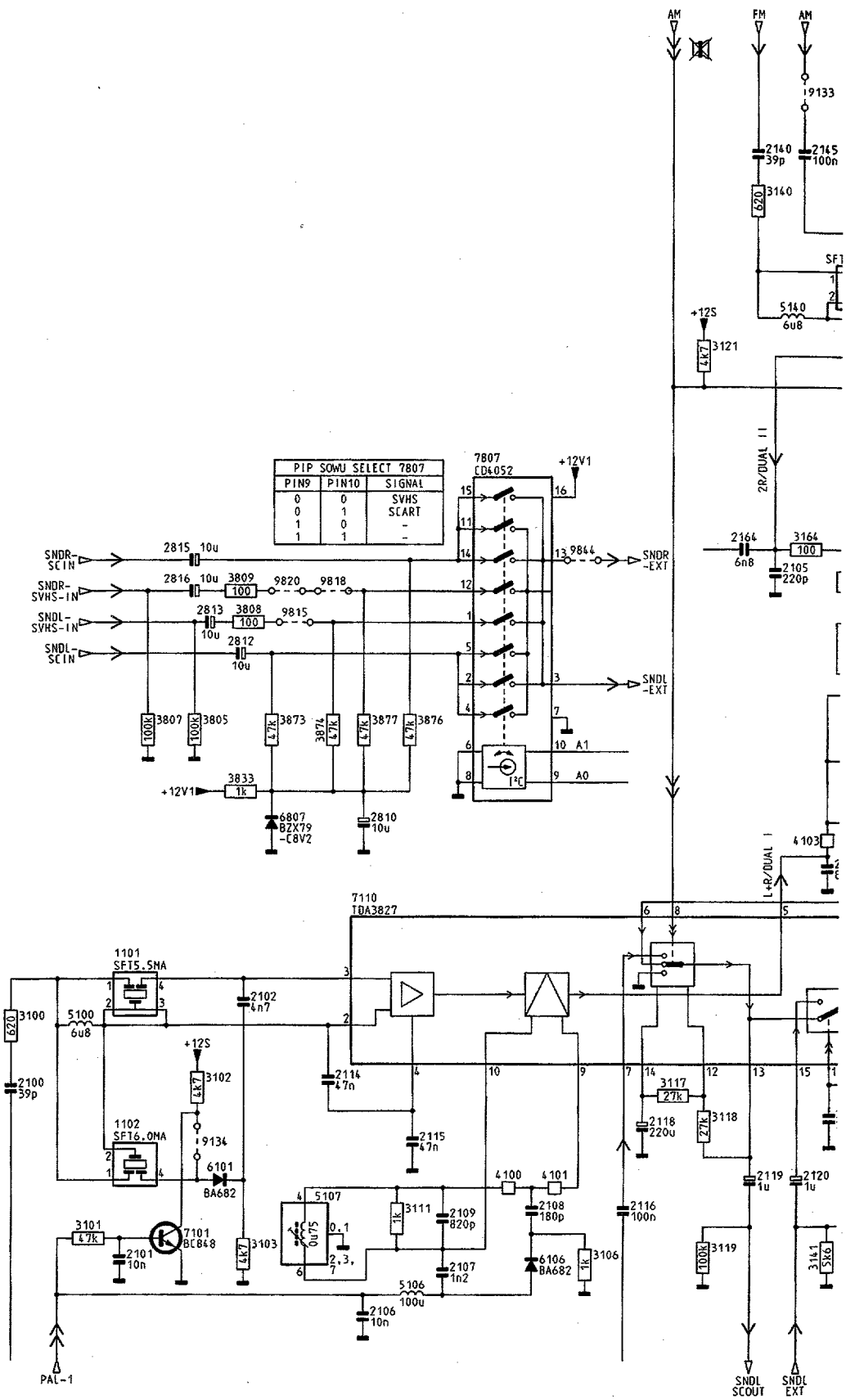
Source selection and volume adjustment

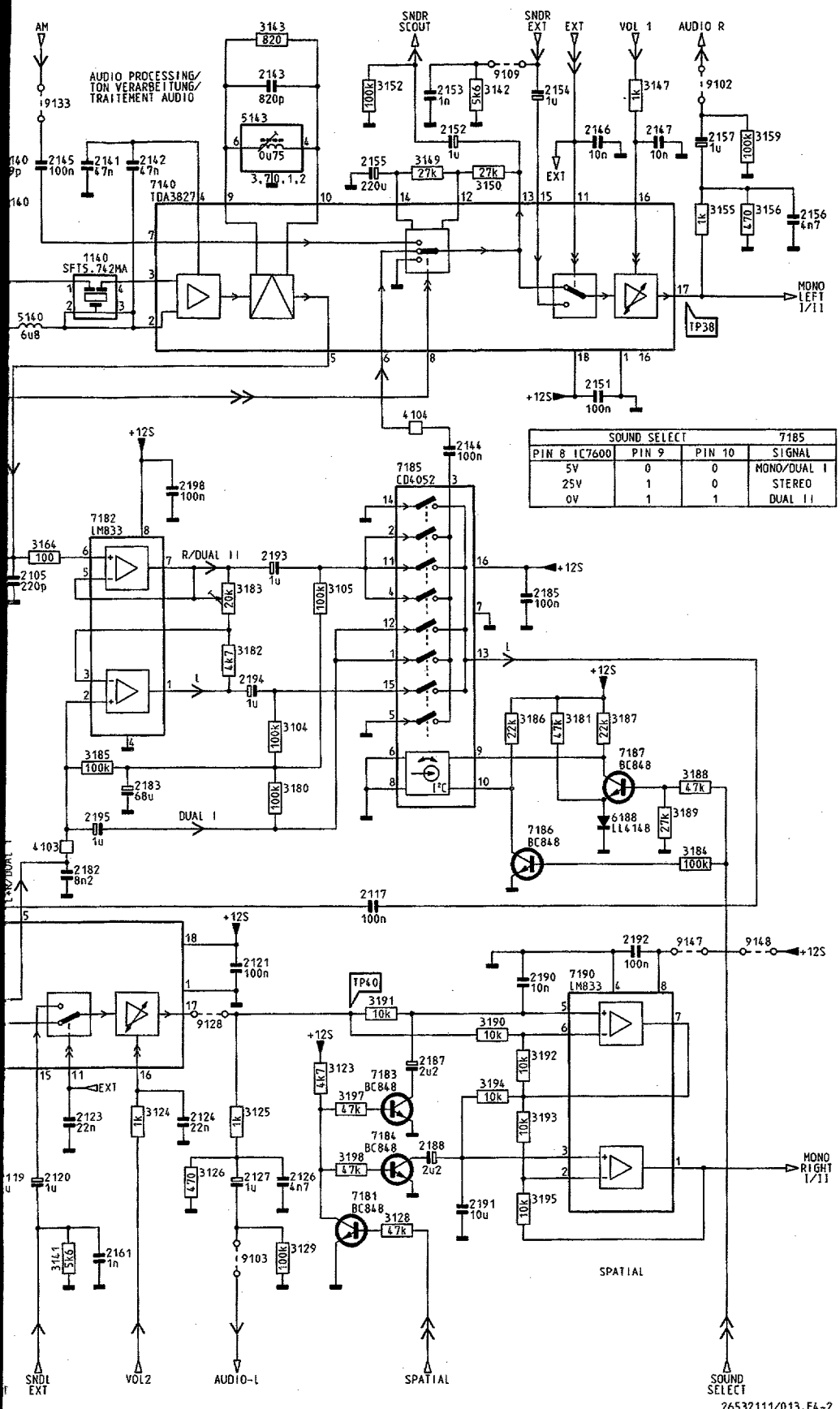
Following a choice for sound from the Euro connector (pin 11) or TV reception, the signal is fed via an amplifier and a source selection switch to an adjustable amplifier where the volume can be adjusted using the voltage on pin 16.
The output signal on pin 17 is shorted to earth by TS7103 when the set is switched on to avoid switching sounds.



26532111/013,F4-1

.1


AM
FM
AM
9133
2140 39p
2145 100n
620 3140
SF1
5140 6u8
+12S
4k7 3121
2R/DUAL II
PIP SOWU SELECT 7807
PIN9 PIN10 SIGNAL
0 0 SVHS
0 1 SCART
1 0 -
1 1 -
7807 CD4052
+12V1
SNDR-SCIN
SNDR-SVHS-IN
SNDL-SVHS-IN
SNDL-SCIN
2815 10u
2816 10u
3809 100
9820
9818
2813 10u
3808 100
9815
2812 10u
9844
SNDR-EXT
SNDL-EXT
2164 6n8
3164 100
2105 220p
3807 100k
3805 100k
3873 4k7
3874 4k7
3877 4k7
3876 4k7
A1
A0
I²C
3833 1k
6807 BZX79-C8V2
2810 10u
4103
L+R/DUAL I
7110 TDA3827
1101 SFT5.5MA
3100 620
5100 6u8
2102 4n7
2100 39p
+12S
3102 4k7
1102 SFT6.0MA
9134
6101 BA682
2114 47n
2115 47n
3117 27k
2118 220u
3118 27k
2119 1u
2120 1u
4100
4101
5107 0u75
0,1
2,3,7
3111 1k
2109 820p
2108 180p
2116 100n
3101 47k
7101 BC848
2101 10n
3103 4k7
2107 1n2
6106 BA682
3106 1k
5106 100u
2106 10n
3119 100k
3141 5k6
PAL-1
SNDL SCOUT
SNDL EXT



SOUND SELECT			7185
PIN 8 IC7600	PIN 9	PIN 10	SIGNAL
5V	0	0	MONO/DUAL I
25V	1	0	STEREO
0V	1	1	DUAL II

Fig. 4.2

Sound choice

IC7185 makes it possible to choose between mono, stereo, language I and language II. This choice must be made by the user (language choice on the remote control). On the operation of this key the remote control generates a voltage of 0V, 2.5V, or 5V on the sound select line, which in turn selects mono/language I, stereo and language II respectively.

Source selection

In sets with an interface module it is possible to select the sound belonging to the picture signal being received at that time with IC 7807 (CD4052).

2nd carrier wave detection (Fig. 4.3)

The demodulation signal of an eventual 2nd carrier wave (pin 5/IC 7140), is supplied to transistor TS7165, which together with TS7170 amplifies this signal, following which it is rectified by D6107. Differential amplifier TS7173/TS7174 forms a voltage comparator which compares the rectified voltage on the cathode of D6107 with the reference voltage of the voltage levels of TS7111 and TS7175. If the voltage on the base of TS7173 reaches a specific value, a signal is available on the 2nd carrier wave, TS7112 will cease conducting, resulting in the microcomputer receiving the signal '2nd carrier wave present'.

The output amplifiers (Fig. 4.4)

IC 7130 and IC 7160 are the output amplifier IC's, each with a nominal output power of 1 Watt. These are output amplifiers with two outputs switched in opposing phase (bridge circuit), between which the loudspeakers can be connected.
With switch SN1 a choice can be made between internal and external loudspeakers. When headphones are connected the signal to the loudspeakers is cut off.

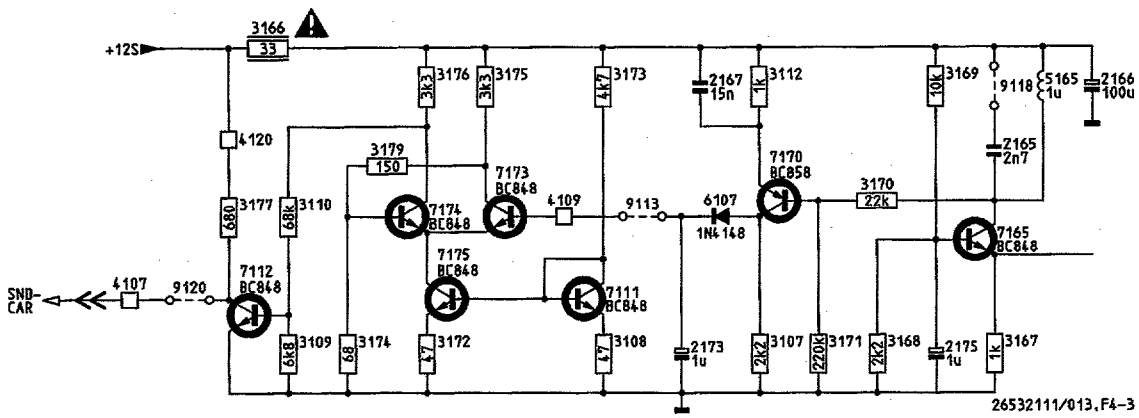


Fig. 4.3

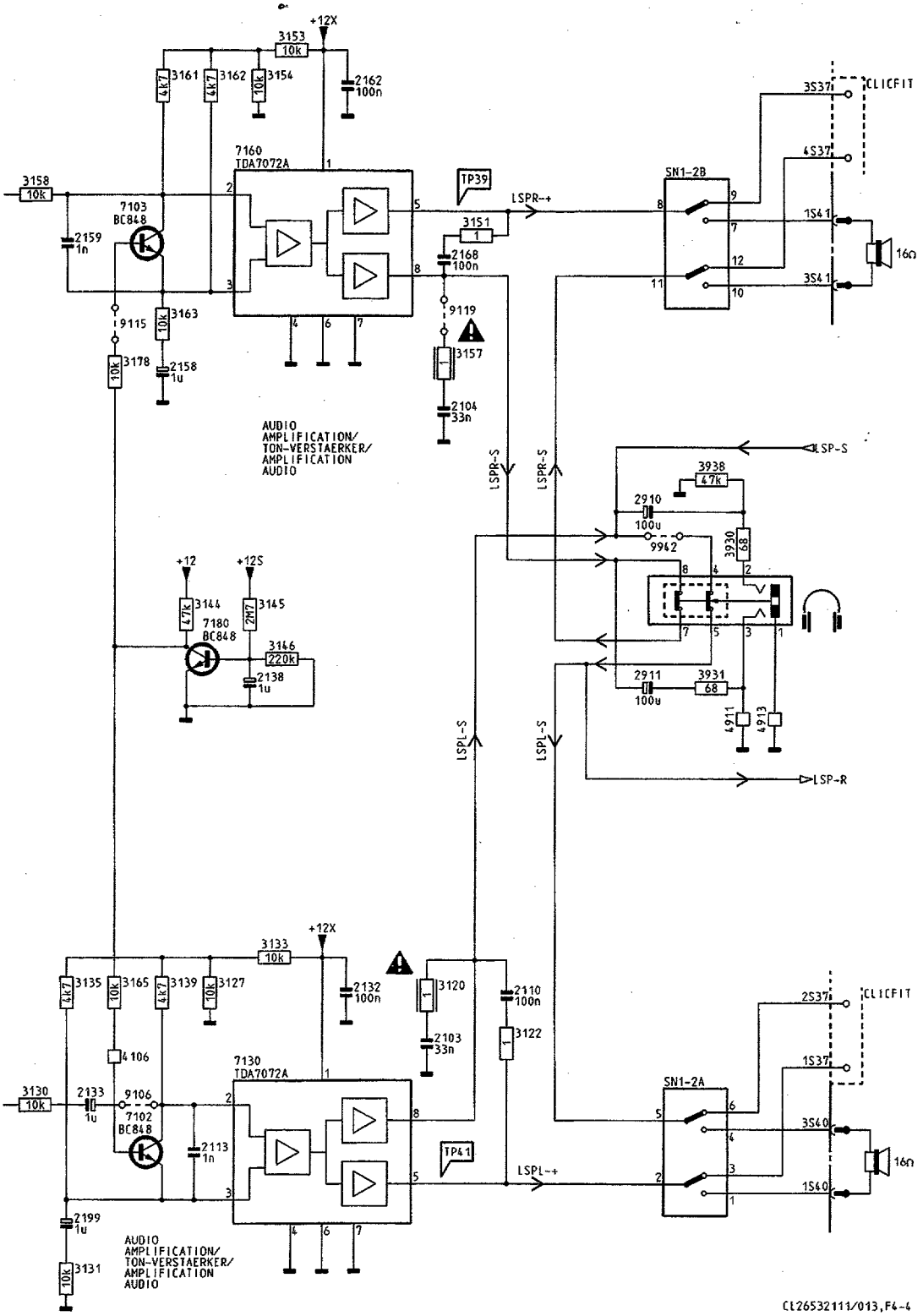

+12X
3153 10k
4k7 3161
4k7 3162
10k 3154
2162 100n
7160 TDA7072A
3158 10k
7103 BC848
2159 1n
9115
10k 3163
10k 3178
2158 1u
TP39
LSPR-+
3151 1
2168 100n
9119
3157
2104 33n
SN1-2B
3S37
CLICFIT
4S37
1S41
16Ω
3S41
AUDIO AMPLIFICATION/ TON-VERSTAERKER/ AMPLIFICATION AUDIO
LSPR-S
LSP-S
3938 47k
2910 100u
9942
3930 68
+12
+12S
47k 3144
2M7 3145
7180 BC848
3146 220k
2138 1u
2911 100u
3931 68
4911
4913
LSPL-S
LSP-R
3133 10k
4k7 3135
10k 3165
4k7 3139
10k 3127
2132 100n
3120 1
2110 100n
2103 33n
3122 1
4106
7130 TDA7072A
3130 10k
2133 1u
9106
7102 BC848
2113 1n
TP41
LSPL-+
SN1-2A
2S37
1S37
3S40
1S40
16Ω
2199 1u
3131 10k
AUDIO AMPLIFICATION/ TON-VERSTAERKER/ AMPLIFICATION AUDIO
CL26532111/013,F4-4

Fig. 4.4

5. Video circuit

Contents

5.1 Source selection (Fig. 5.1)

In sets without an interface module the CVBS signal from the tuner goes directly to the brightness and chrominance circuits.
In sets with an interface module the source selection switch (IC 7805) selects one of the video signals being offered. This could be the CVBS from the tuner (pin 5), CVBS from the Euro connector (pin 2) or luminance from the SVHS input (pin 1). The selected signal (pin 3) is amplified by TS7813 and TS7826 and is distributed over the luminance circuit (via TS7809) and the chrominance circuit (via IC 7803).
IC 7803 normally switches the chrominance-CVBS signal through to the further chrominance processing. For SVHS signals transistor TS7812 is switched to conduct. Pin 3 IC 7803 then goes low and the SVHS chrominance signal that is supplied via pin 4 is selected.

PIP source selection

Using the source selection switch for the PIP picture (IC 7806), a choice can be made from the CVBS signals from the tuner (pin 14), the euro connector (pin 15) or the SVHS input (pin 12). The SVHS signal is converted to a CVBS for this purpose. Filter 5800 first filters the 4.43 MHz components from the Y-signal following which the brightness and chrominance are added together via R3879 and R3862.

Source selection control

The source selection switches are controlled by the microcomputer via IC 7804. This is an IC controlled IC from which output pins 4,5,6,7,10 and 11 can be made low or high as required. These outputs control the various selection IC's (IC 7805 IC 7806 and IC 7807).

5.2 Luminance circuit (Fig. 5.2)

The CVBS/SVHS-Y signal selected for the luminance circuit are delayed by 500nS by delay line 5251. This enables the luminance and chrominance signals to be simultaneously available on the video adjuster IC 7280 (TDA3504). In sets without SVHS the luminance signal is also filtered by a chrominance band stop filter in 5251. In sets with SVHS this filtering is performed by filter 5280, which on reception of SVHS signals is switched out via TS5285.

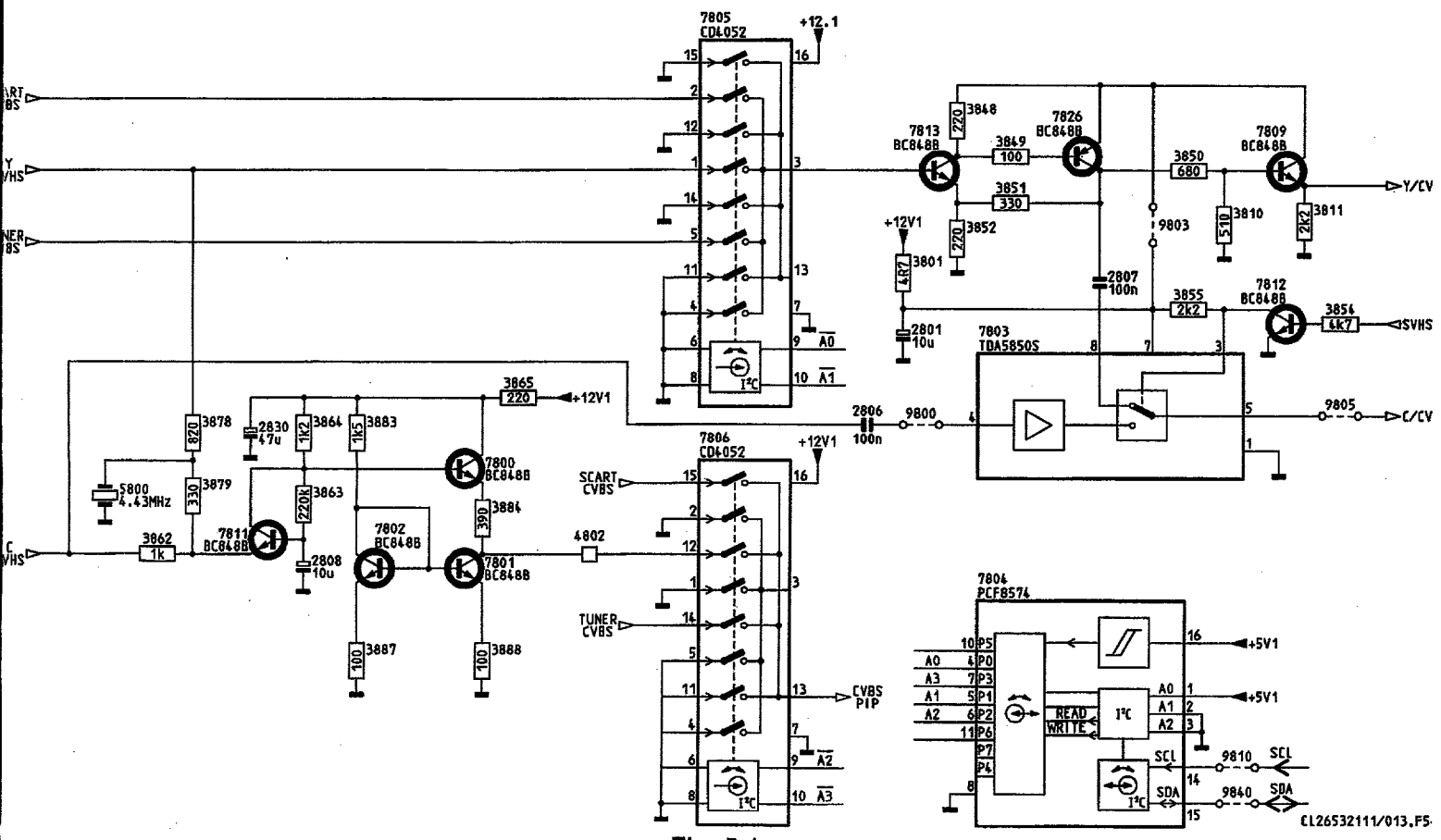


Fig. 5.1

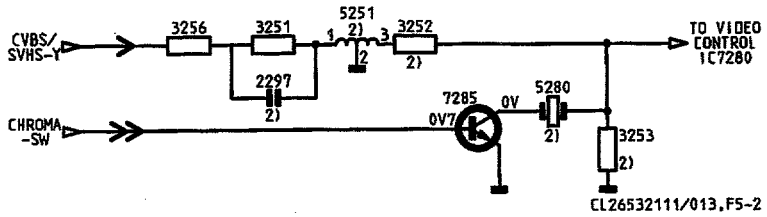

CVBS/
SVHS-Y
3256
3251
5251
2)
3252
2)
TO VIDEO
CONTROL
IC7280
2297
2)
CHROMA
-SW
7285
0V7
0V
5280
2)
3253
2)
CL26532111/013,F5-2

Fig. 5.2

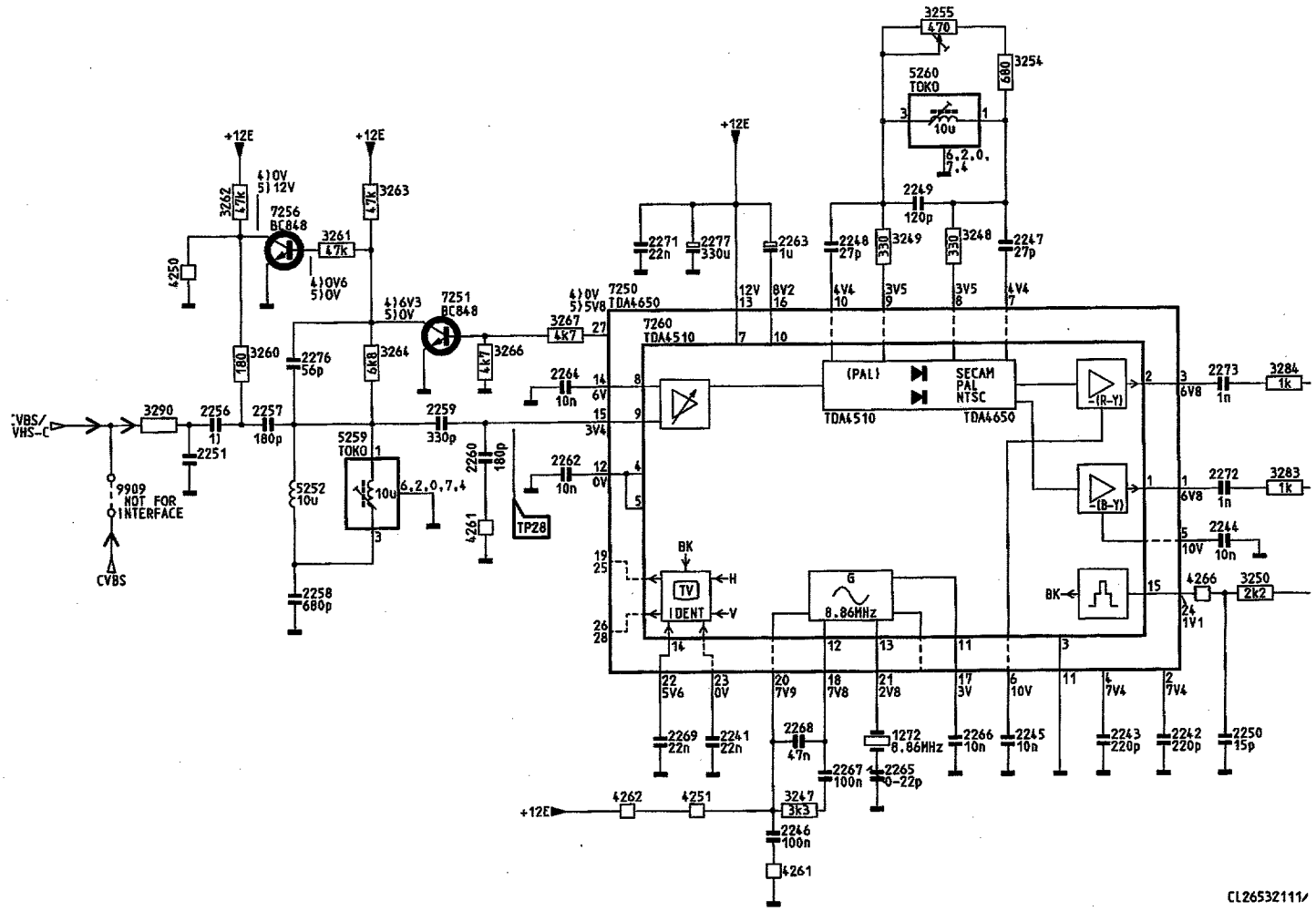

3255
470
3254
680
5260
TOKO
10u
6.2.0.
7.4
+12E
2249
120p
2271
22n
2277
330u
2263
1u
2248
27p
3249
3248
2247
27p
7250
TDA4650
7260
TDA4510
(PAL)
SECAM
PAL
NTSC
TDA4510
TDA4650
-(R-Y)
-(B-Y)
2273
1n
3284
1k
2272
1n
3283
1k
2244
10n
4266
3250
2k2
BK
TV
IDENT
H
V
8.86MHz
3262
4k7
7256
BC848
3261
4k7
3263
4k7
4250
7251
BC848
3267
4k7
3266
4k7
3260
180
2276
56p
3264
6k8
2264
10n
2262
10n
3290
2256
1)
2251
2257
180p
2259
330p
2260
180p
5259
TOKO
10u
6.2.0.7.4
5252
10u
2258
680p
4261
TP28
9909
NOT FOR
INTERFACE
CVBS
VBS/
VHS-C
2269
22n
2241
22n
2268
47n
1272
8.86MHz
2267
100n
2265
6-22p
2266
10n
2245
10n
2243
220p
2242
220p
2250
15p
4262
4251
3247
3k3
2246
100n
4261
CL26532111/

Fig. 5.3

5.3 Chrominance circuit (Fig. 5.3)

The selected chrominance signal (CVBS/SVHS-C) is supplied to IC 7250 (TDA4650) or IC 7260 (TDA4510) via an input filter.
IC 7260 is only used in sets suitable for the reception of PAL signals, whilst IC 7250 is used in sets suitable for the reception of both PAL and SECAM signals.

The CVBS signal is fed to a chrominance band-pass filter. In case of a set only suitable for PAL reception this is formed by coil 5252 and capacitor 2258. This filter is tuned to 4.43 MHz.

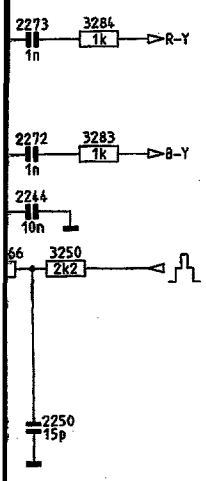
In case the set is suitable for PAL and SECAM reception the filter is supplemented with transistor 7251 and coil 5259. In case of PAL signal recognition 7251 is isolated, resulting in a band-pass filter which is built exclusively around coil 5259 and capacitor 2258. This is tuned to 4.43 MHz.

On SECAM signal recognition 7251 is set to conduct. The filter formed by SECAM has an anti-clockwise curve with its peak at 4.286 MHz. This is adjusted with L5259.

PAL chrominance decoder IC 7260

The PAL chrominance signal is offered to pin 9 of IC 7260. This signal is demodulated and decoded to the basic band B-Y and R-Y signals which are available on pins 2 and 1 respectively of IC 7260.

PAL/SECAM chrominance decoder IC 7250



The chrominance signal (PAL, SECAM) is offered to pin 15 of IC 7250.
The system being received is recognized on the basis of the colour "burst" (in case of PAL) or the identification signal (in case of SECAM) on the last step of the CVBS signal.

The identification circuit in IC 7250 recognizes these signals and goes high if a SECAM signal is being received. This causes the switching of the input filter via transistor 7251.

Service tip:

By connecting +12V to one of the two following points (pin 27 for SECAM, pin 28 for PAL) sets IC 7250 in the system required. This can be used to simplify fault finding. The identification circuits described earlier are bridged in this manner.

Base band delay line (Fig. 5.4)

The B-Y and R-Y signals coming from the chrominance decoder are fed to the base band delay line in IC 7290 (TDA4661). The direct and one-line time delayed signal are then added together.

The corrected B-Y and R-Y signals are fed to the video controller IC 7280 (TDA3504).

5.4 The video controller (Fig. 5.5)

The Video controller IC dematrixes R-Y, B-Y and Y signals in R,G, and B signals. The colour saturation (pin 12) is actually adjusted first. The mixed external, PIP, and TXT-RGB signals are received on pins 8, 9 and 10 and are selected by the fast blanking on pin 7. Subsequently, the luminance (pin 17) and contrast (pin 16) are adjusted. There is also a beam-current limiter (TS7281) present. The output signals are RGB signals (pins 1,19,20) that control the RGB output amplifiers on the picture tube panel.

RGB inputs

The RGB input signals from the Euro connector go first to the PIP module in sets with PIP, are mixed with the teletext RGB signals and then go to the video controller (IC 7280) sandcastle pulse.

The sandcastle pulse synchronises colour decoding, the luminance and chrominance signal processing and correlates the RGB signals to the raster.

5.5 RGB output amplifiers (Fig. 5.6)

The RGB output amplifiers consist of 3 identical class A amplifiers built up around transistors 7205, 7218 and 7227.

Peak beam current limiter

The peak beam current information (EHT info) is measured via diode 6289 to prevent any overloading of the picture tube and the main high voltage power supply. This limitation is achieved by adjusting back the contrast voltage of IC 7280. Due to this limiter the contrast voltage always remains lower than 4 volts.

High voltage, Focus & VG2

The high voltage and the focus and VG2 voltages are supplied by the line output stage. The focus and VG2 can be adjusted by means of the potentiometers on the line transformer 5445.

Picture tube flash-over protection

To protect the receiver against picture tube flash-over the following precautionary measures have been taken:

1) spark gaps (3,7,9) on all electrode connections on the picture tube panel.
2) resistors in series with RGB electrodes (3203, 3216, 3229).

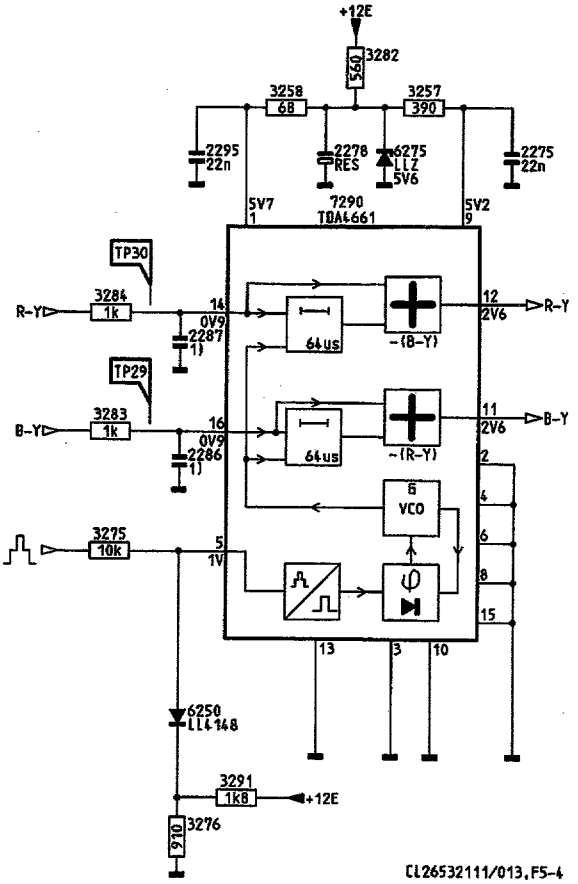

+12E
3282
560
3258
68
3257
390
2295
22n
2278
RES
6275
LLZ
5V6
2275
22n
5V7
1
7290
TDA4661
5V2
9
TP30
R-Y
3284
1k
14
0V9
2287
1)
64us
-(B-Y)
12
2V6
R-Y
TP29
B-Y
3283
1k
16
0V9
2286
1)
64us
-(R-Y)
11
2V6
B-Y
2
4
6
8
15
G
VCO
3275
10k
5
1V
13
3
10
6250
LL4148
3291
1k8
+12E
910
3276
CL26532111/013.F5-4

Fig. 5.4

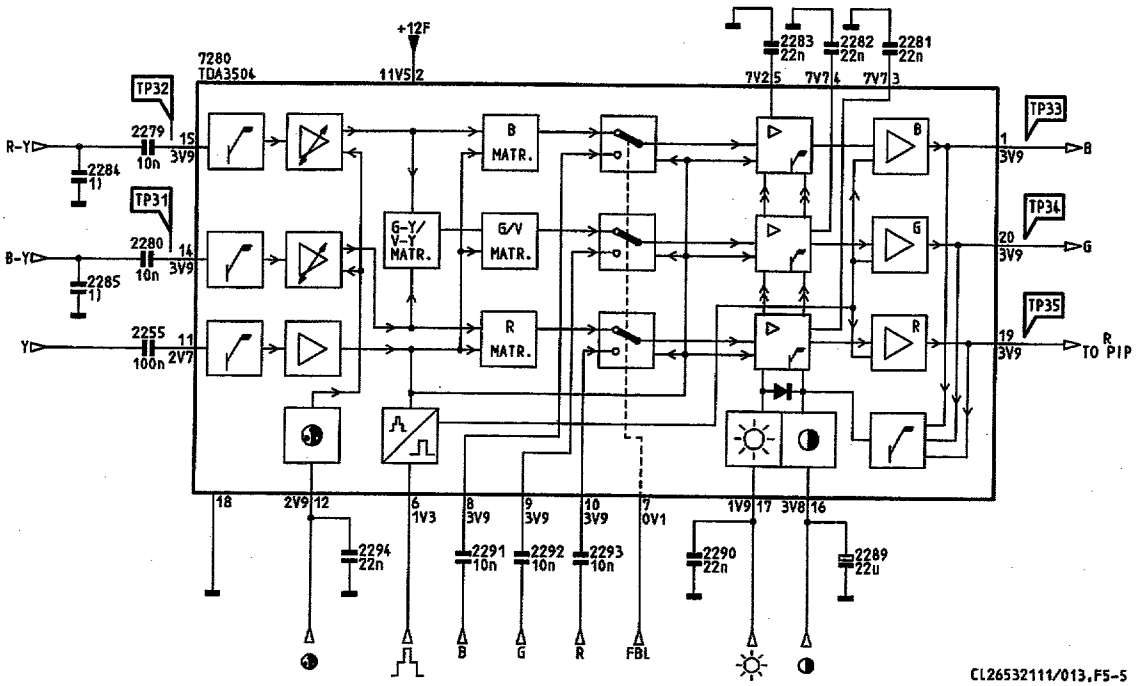

+12F
7280
TDA3504
11V5
2
2283
22n
2282
22n
2281
22n
7V2
5
7V7
4
7V7
3
TP32
R-Y
2279
10n
15
3V9
2284
1)
TP31
B-Y
2280
10n
14
3V9
2285
1)
Y
2255
100n
11
2V7
B
MATR.
G-Y/
V-Y
MATR.
G/V
MATR.
R
MATR.
TP33
1
3V9
B
TP34
20
3V9
G
TP35
19
3V9
R
TO PIP
18
2V9
12
6
1V3
8
3V9
9
3V9
10
3V9
7
0V1
1V9
17
3V8
16
2294
22n
2291
10n
2292
10n
2293
10n
2290
22n
2289
22u
B
G
R
FBL
CL26532111/013.F5-5

Fig. 5.5

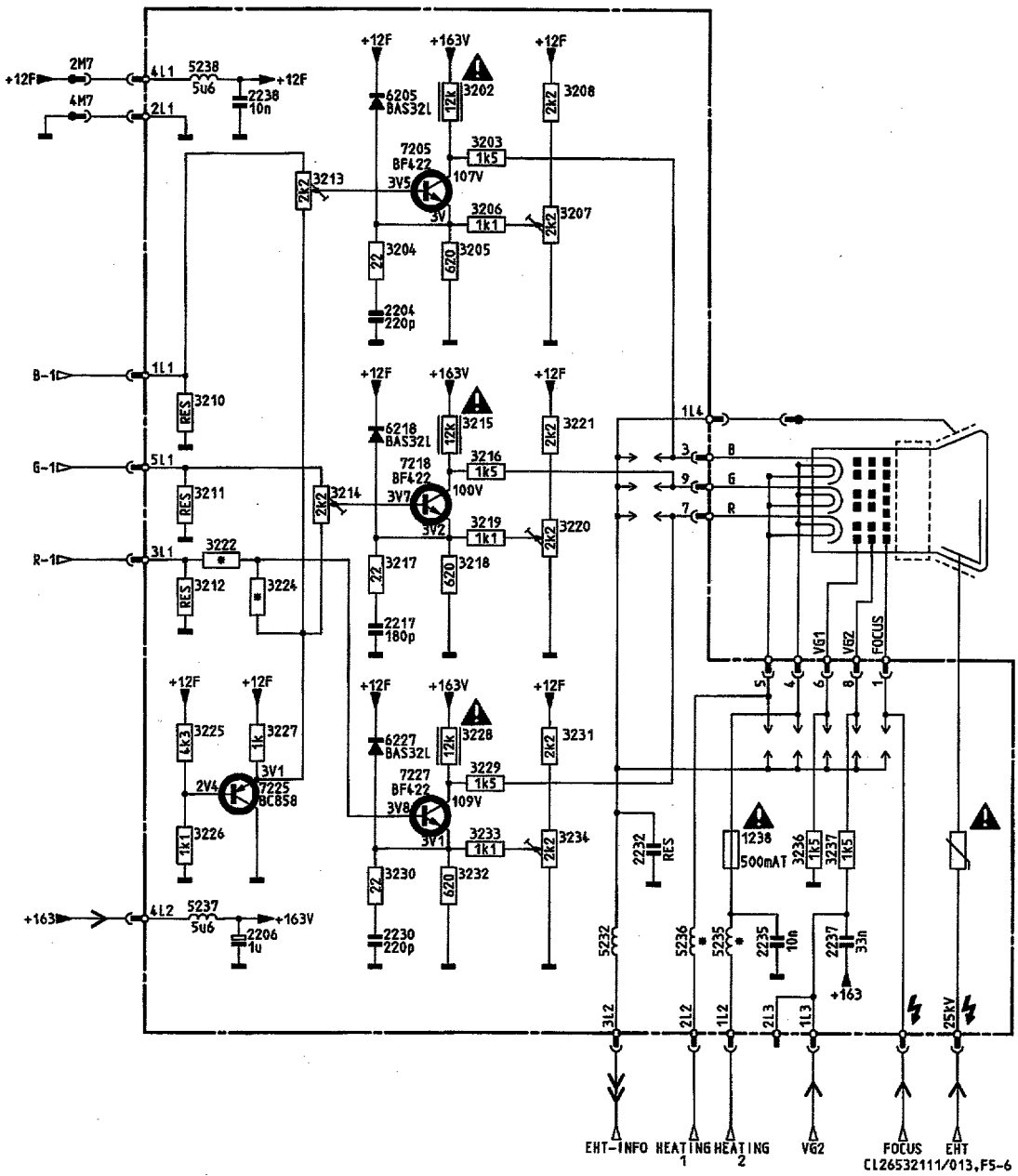

+12F
+163V
2M7
4M7
4L1
2L1
5238
5u6
2238
10n
6205
BAS32L
3202
12k
3208
2k2
7205
BF422
3203
1k5
3V5
107V
3213
2k7
3206
1k1
3207
3204
22
3205
620
2204
220p
B-1
G-1
R-1
1L1
5L1
3L1
3210
RES
3211
3222
3212
3224
6218
BAS32L
3215
3221
7218
BF422
3216
3V7
100V
3214
3219
3220
3217
3218
2217
180p
1L4
3
9
7
B
G
R
VG1
VG2
FOCUS
5
4
6
8
1
6k3
3225
1k
3227
3V1
2V4
7225
BC858
3226
6227
BAS32L
3228
3231
7227
BF422
3229
3V8
109V
3233
3234
3230
3232
2230
220p
+163
4L2
5237
5u6
2206
1u
2232
RES
1238
500mAT
3236
3237
5232
5236
5235
2235
10n
2237
33n
3L2
2L2
1L2
2L3
1L3
25KV
EHT-INFO
HEATING 1
HEATING 2
VG2
FOCUS
EHT
CL26532111/013,F5-6

Fig. 5.6

6. Synchronisation and deflection

Besides the intermediate frequency circuit (IC 7300/2A), IC 7300 (Fig. 6.1) also contains the horizontal and vertical synchronisation circuit and a sandcastle pulse generator (IC 7300/2B).
The CVBS picture signal is fed to pin 28 of IC 7300/2B. Via the synchronisation separator in the IC, the synchronisation signals are fed to the horizontal oscillator, the vertical oscillator and the identification circuit, which on transmitter recognition supplies a "low" signal to pin 14 and a "high" signal to pin 25.

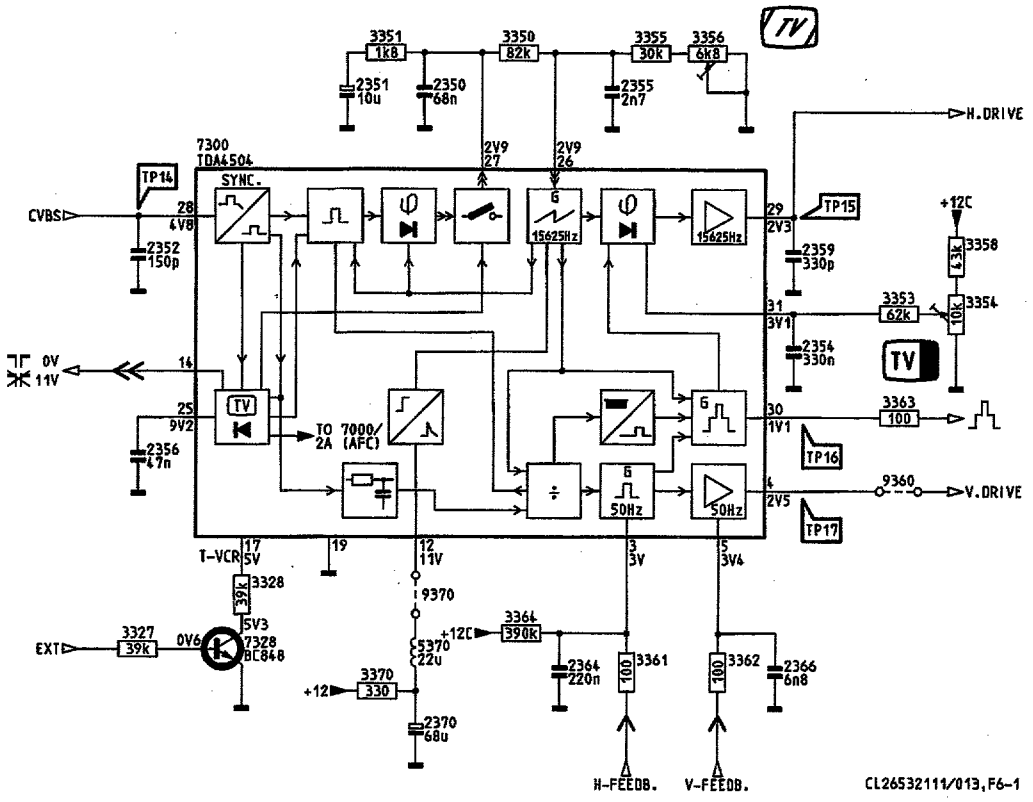


Fig. 6.1

Horizontal synchronisation

The horizontal oscillator is a free running sawtooth generator. The free running frequency is adjusted with the aid of 3356. During the adjustment of 3356 the input (pin 28) should be connected to the 12+C.
If a transmitter is being received, the free running oscillator is synchronised with the synchronisation pulse from the synchronisation separator. The synchronised sawtooth voltage is fed to the output amplifier which supplies a square wave voltage on pin 29, the horizontal control signal.

Horizontal centring

The horizontal centring is adjusted with potentiometer 3354.

Vertical synchronisation

The raster pulse is taken from the synchronisation signals from the synchronisation separator and fed to a circuit which counts the horizontal pulses. After 625 lines a raster pulse is generated. The vertical control signal, which is synchronised with the horizontal and vertical flyback pulses, is available on pin 4 of IC 7300.

Sandcastle

The sandcastle pulse generator generates the sandcastle signal with the aid of the horizontal and vertical pulses and is available on pin 30 of IC 7300

Horizontal deflection (Fig. 6.2)

The horizontal control signal controls the line output stage, transistor 7445 and line transformer 5445 via transistor 7440 and transformer 5441.
The line output stage supplies the horizontal deflection current and various power supply voltages.
The horizontal flyback signal is taken off the secondary side of transformer 5445 (pin 7).

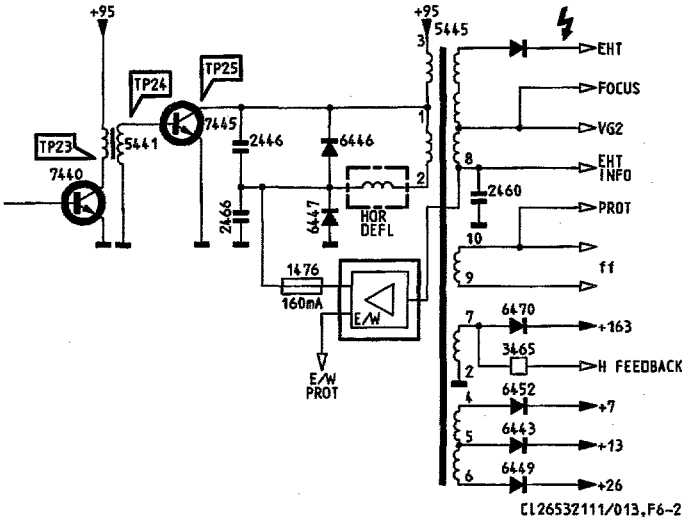


Fig. 6.2

Vertical deflection (Fig. 6.3)

The vertical deflection is provided by IC 7400 (TDA3653). Pins 1 and 3 of this IC are fed with the vertical control signal from IC 7300/2B and generates a deflection current on pin 5.

The vertical centring is determined by the current fed to resistor 3401. A choice from 3 adjustments can be made using switch 1401. The picture amplitude can be adjusted with potentiometer 3410.
The vertical flyback is generated on pin 8 of the IC.

For a detailed description of horizontal and vertical deflection please refer to the circuit description of chassis GR1-AX.

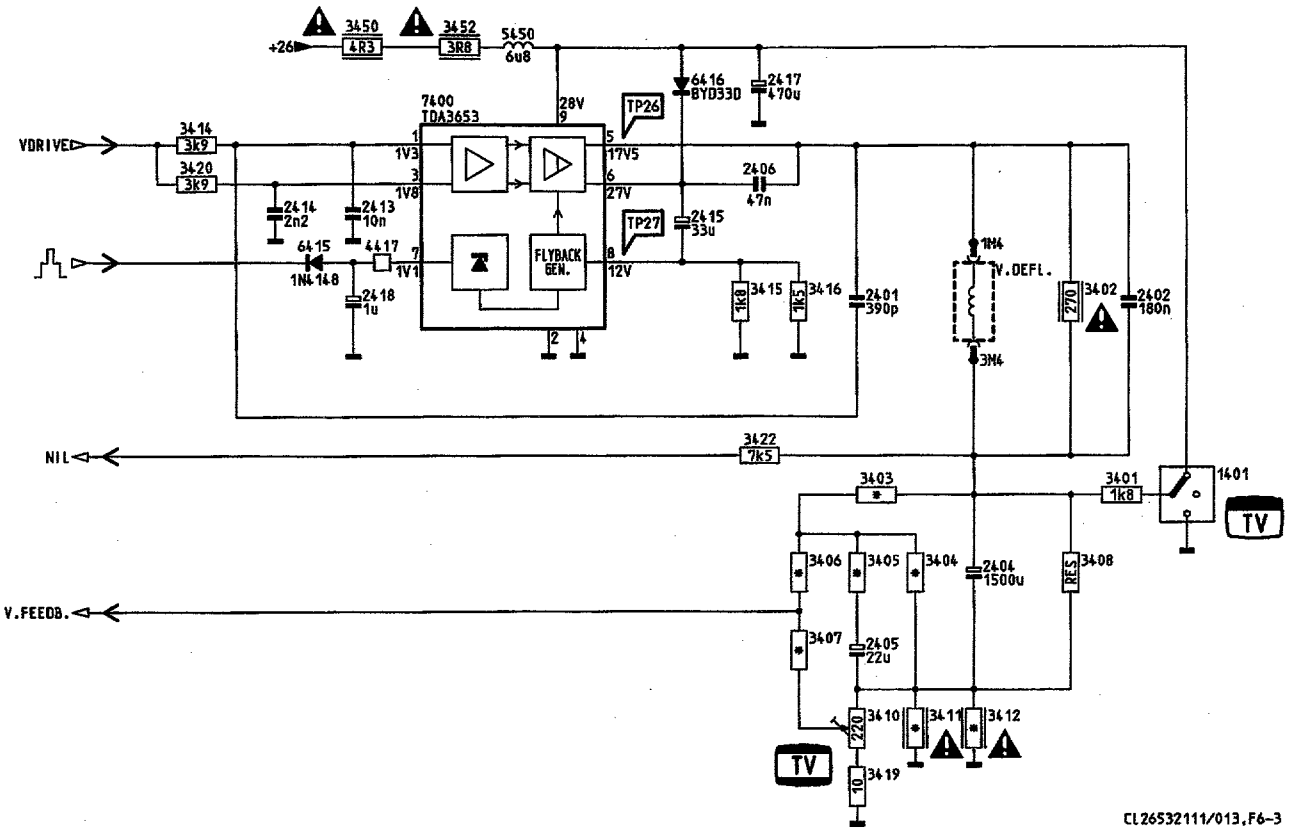

+26
3450
4R3
3452
3R8
5450
6u8
7400
TDA3653
28V
9
TP26
6416
BYD33D
2417
470u
VDRIVE
3414
3k9
3420
3k9
1V3
1V8
17V5
27V
2406
47n
2414
2n2
2413
10n
2415
33u
TP27
6415
1N4148
4417
1V1
FLYBACK
GEN.
12V
2418
1u
1k8
3415
1k5
3416
2401
390p
1N4
V.DEFL.
3M4
270
3402
2402
180n
NIL
3422
7k5
3403
3401
1k8
1401
TV
3406
3405
3404
2404
1500u
RES
3408
V.FEEDB.
3407
2405
22u
220
3410
3411
3412
10
3419
TV
CL26532111/013.F6-3

Fig. 6.3

7. Teletext (Fig. 7.1)

Teletext

The teletext module is fed by the +7V power supply from the line output stage, and is controlled with the CVBS signal from the intermediate frequency IC 7300.

The teletext decoder is build around IC 7700 (SAA5246), in which the previously used video processor and the character generator are combined. A separate microcomputer (IC 7702) is used to control the decoder. In addition to standard teletext the SAA5256 can also decode the expanded teletext system TOP (Table of Pages) and FLOF (Full Level One Features).
The SAA5246 is available in 3 language versions:
SAA5246/E European languages
SAA5246/H Eastern European languages
SAA5224/T Western European languages and Turkish

Communication between the teletext module and the microcomputer on the chassis takes place via the IC bus. Transistors 7755 and 7754 generate a reset signal for the TXT microcomputer on start up.
The selected pages are stored in the RAM memory of IC 7701.

The CVBS/Y signal is fed to the teletext decoder IC 7700(SAA5246) via pin 8. For Scandinavian countries the envelope delay time in the circuit around TS7732 and TS7731 has been modified.
The teletext decoder generates RGB teletext signals (pins 15, 16 and 17), a fast blanking signal (pin 19), a non-interlace signal (pin 21) and a contrast control signal (pin 20).

Detailed description

For more information concerning the operation of the teletext circuit please refer to the previously published circuit description 'Computer Controlled Teletext (CCT)'.

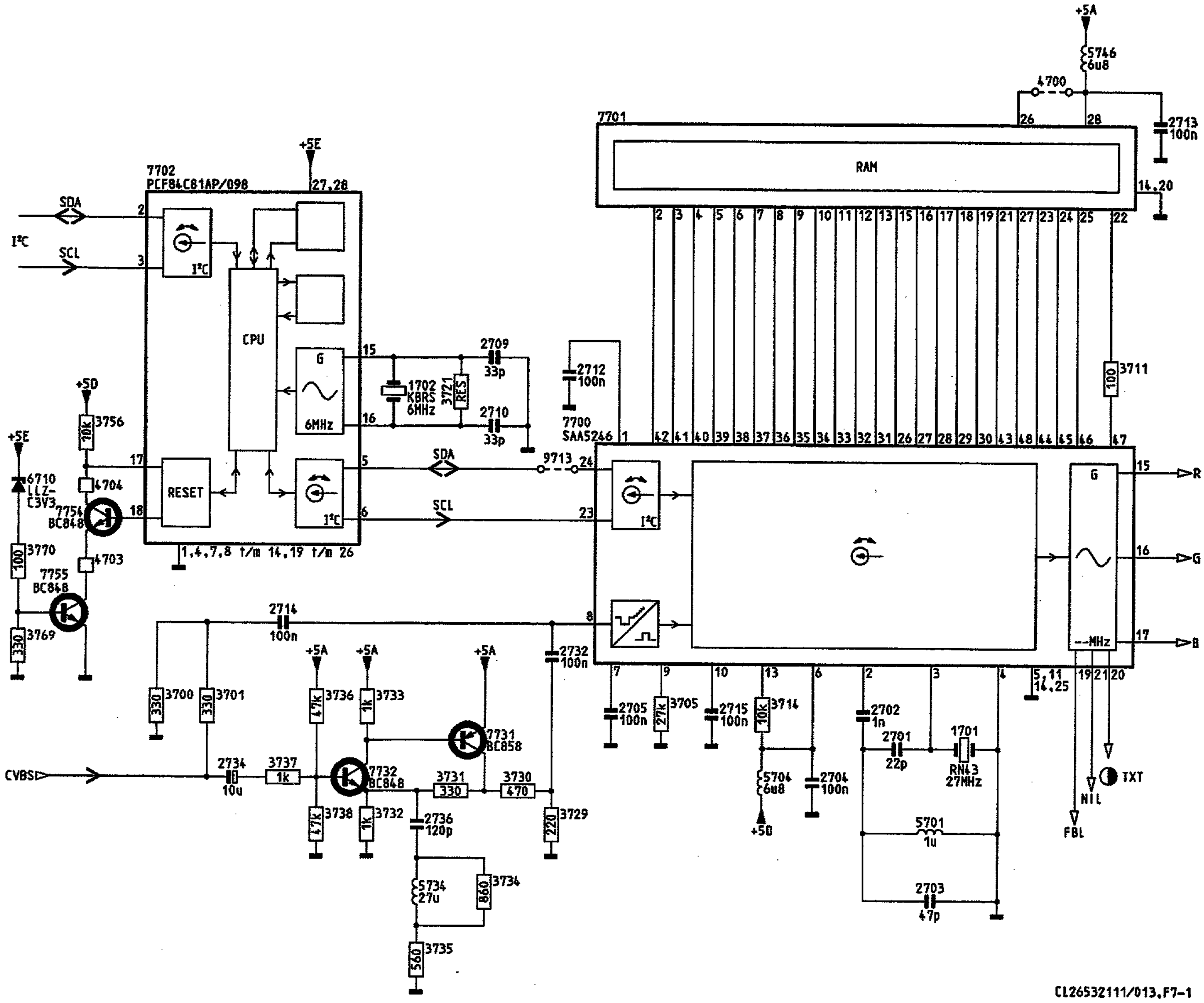

7701
RAM
7702
PCF84C81AP/098
CPU
RESET
6MHz
7700
SAA5246
SDA
SCL
I²C
CVBS
+5E
+5D
+5A
1702
KBRS
6MHz
1701
RN43
27MHz
R
G
B
FBL
NIL
TXT
CL26532111/013.F7-1

Fig. 7.1

8. PIP

Contents

8.1 Introduction

PIP is the abbreviation for Picture In Picture. This is a second picture, reduced, with limited picture sharpness, projected in the large picture. In order to look at another programme in this small picture, it is necessary to connect at least one other external source. The source which is made visible in the small picture gives no sound information. The sound information always comes from the large picture.

PIP dimensions

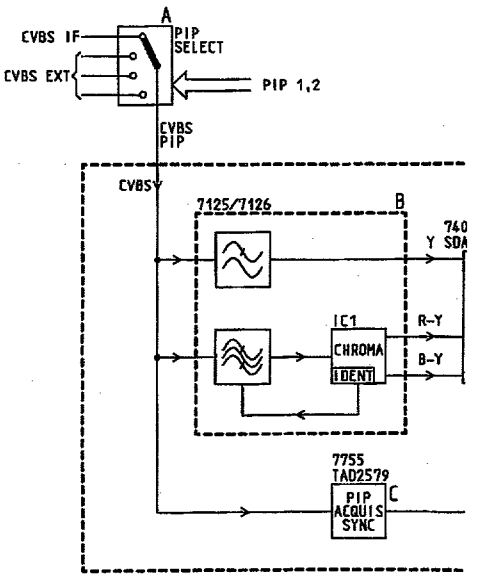
A choice can be made between two formats of the PIP picture (1/9 or 1/16 of the main picture). Depending on this, the PIP picture contains more or fewer lines.

PIP framework

There is a frame around the PIP picture. The frame thickness above and below is equal to 4 lines. The frame thickness on the left and right is equal to 0.5µs.

Picture reduction

Only a limited part of the total video signal supplied is used for the PIP acquisition, namely 264 lines, and 47 µs of each line.
The picture is reduced linearly 3 times (4 times with large 1/16). This picture reduction is obtained by averaging picture lines and picture elements. See also section 8.6.



Fig

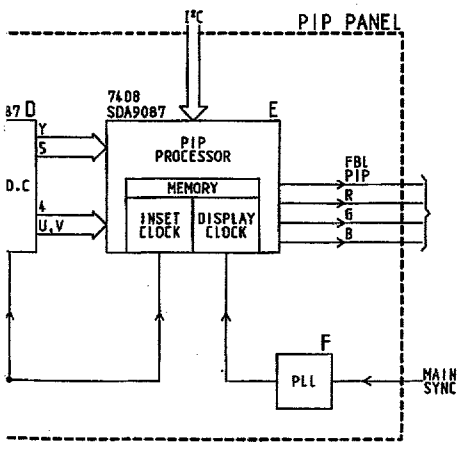
8.2 The block diagram

In the PIPSELECT part (A) it is determined which signal is shown in the PIP picture; this part is on the EURO module (see also section 5.2 Video source selection).

The PIP CVBS signal selected goes to the PIP panel. The CVBS signal is supplied here to the luminance-chrominance part (B) and to the synchronisation part (C). The chrominance signal is separated from the luminance signal and then demodulated, after which both the chrominance and the luminance signal are converted from analog to digital in the D/A converter (D). Depending on the PIP size selected, the digitised signals are then reduced by a factor of 1:16 or 1:9 and stored in the memory of the PIP processor (E).

Because the second signal source is not synchronous with the main signal source, the signal processing described should by synchronous with the main picture. In order to achieve this, a separate synchronisation part (C) is added which supplies signals which are synchronised with the PIP input signal.

The digital Y, U and V signals stored in the memory are read out and converted to R, G and B signals. In order to obtain a stable PIP picture within the main picture, this must be read out synchronised with the synchronisation signals of the main picture.
This synchronisation is obtained by controlling the PLL (F), which activates the read-out clock, with the horizontal synchronisation signal of the main picture.
A PIP fast-blanking signal (FBL PIP) is also controlled by the R, G, B signals if a signal is present from the PIP processor which produces switching between EXT RGB (from EXT1) and PIP RGB.
The RGB output signals, coming from the PIP module, are supplied to the IC7309 (see section 5.5).



CL26532111/013.F8-1

3.1

8.3 PIP Chrominance/luminance path

The PIP-CVBS signal comes in on the basis of TS7234 (see fig. 8.2). The emitter signal branches off and goes to the PIP synchronisation IC (IC7755). The amplified signal present on the emitter of TS7233 is separated into a luminance and a chrominance signal. The luminance signal goes to the ADC SDA9087 (IC7406) after a lowpass filter. In the case of a single-system unit, the chrominance signal goes to the PAL decoder IC7126. In the case of multi-system units, the chrominance signal is sent to the multi-standard decoder IC7125.

PAL only PIP

The chrominance signal is supplied to pin 9 of IC7126 (TDA4510) via a bandpass filter. Colour demodulation takes place in this IC. For further information on the operation of this IC , see section 5.4.

Multi-system PIP

In the case of multi-system PIP, the chrominance signal is supplied to pin 15 of IC7125 (TDA4554) via a bandpass filter. The filter can be switched and has 3 positions:

-SECAM In the SECAM position pins 25, 26 and 28 of IC7125 are low. The input filter now fulfils the circuit clock required for SECAM.

-PAL Pin 28 of IC7125 is now high, the filter is now tuned to 4.43 MHz.

-NTSC NTSC PIP is not used in chassis GR2.1.

System identification

IC7125 (TDA4554) automatically switches one of the colou systems on and checks at the same time pins 25 to 28 for the switching of the input filter. The systems are recognised by the burst or identification signal on the back porch. The identification recognises these signals and then makes one of the output points 25 to 28 high.
Pin 23 is earthed, which means that SECAM line identification is used.

The colour difference signals B-Y and R-Y from the demodulator (IC7125 or IC7126) are supplied to pins 18 and 17 of the A/D converter, respectively.

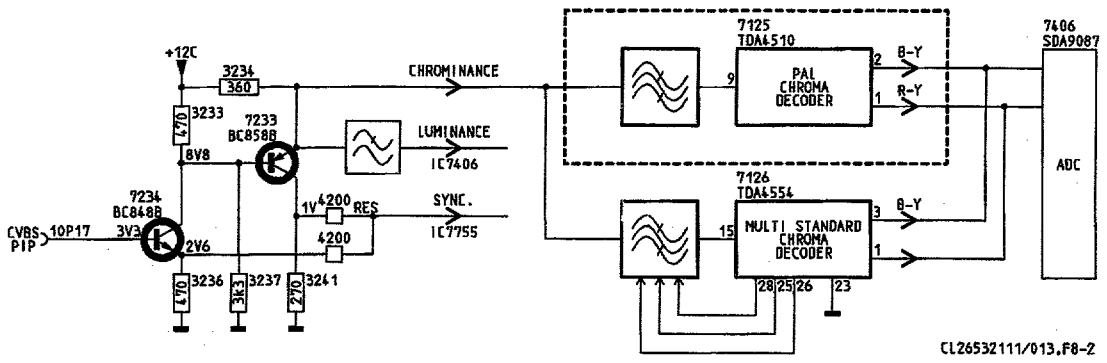


Fig. 8.2

8.4 PIP Synchronisation

Two synchronisations are necessary to process a PIP picture: (see fig. 8.3)

Acquisition Synchronisation

After processing the PIP picture selected is stored in a memory in the PIP processor (IC7408). Synchronisation with the PIP picture is necessary for this. For this a separate synchronisation IC (TDA2579A) is used. This so-called acquisition synchronisation is used in:

- the chrominance part, where the burst key pulse is used to separate burst and chrominance;
- the analog-to-digital converter (A.D.C.), where the burst key is used for clamping, and where a 13.5 MHz clock is produced which is synchronised with the burst key pulse
- the PIP processor, where the READIN clock is activated which is controlled by the horizontal synchronisation and the 13.5 MHz clock of the A.D.C. and by the vertical synchronisation pulses from the acquisition sync. IC.

Display synchronisation

The display of the PIP on the screen must be synchronised with the main picture. The signals for the reading out of the memory of the PIP processor are therefore synchronised with the horizontal and vertical synchronisation pulses of the main picture (display sync).

Aquisition synchronisation IC (TDA2579)

The CVBS PIP comes in at point 5 of IC7755 (see fig.8.4). The horizontal oscillator is built up around the C2238, R3238 and R3239 connected to pin 15. Capacitor C2238 is charged with a constant current from the IC7755 to 6 volts and then discharged via R3238 and R3239. By varying the value of R3239, the discharge time, and thus the frequency, can be varied. In order to set the free-running frequency, the input signal can be short-circuited at point 5. The oscillator is now free and this frequency can be adjusted until the picture is stil with R3239.

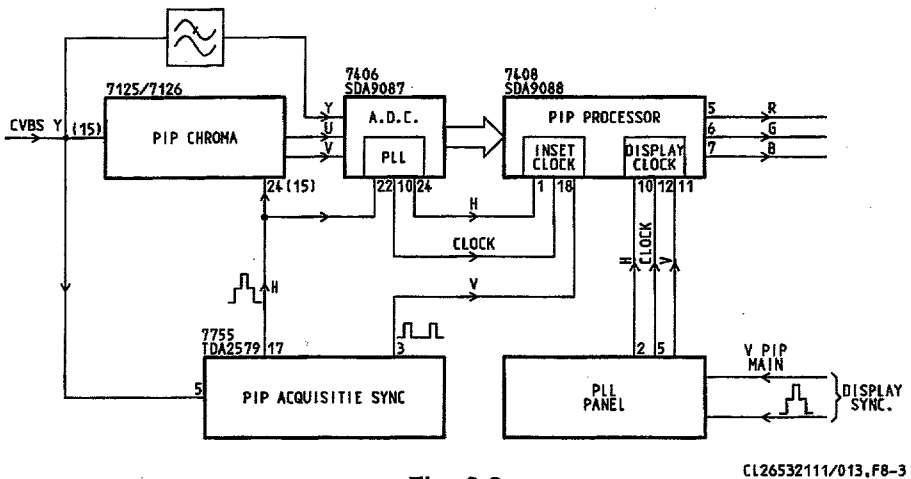


Fig. 8.3

Vertical synchronisation

De vertical synchronisation pulses (V) come to the outside via point 3 and are sent to the PIP processor.

Sandcastle generator

The line pulses supplied by the oscillator (G) go to the sandcastle generator via an amplifier.
The sandcastle pulse at point 17 has two levels:

- 12 volts during the line flyback
- 2.5 volts during the frame flyback

Because the PIP synchronisation does not control any line output stage, the supply voltage (point 10) and the start voltage (point 16) may be switched on at the same time.

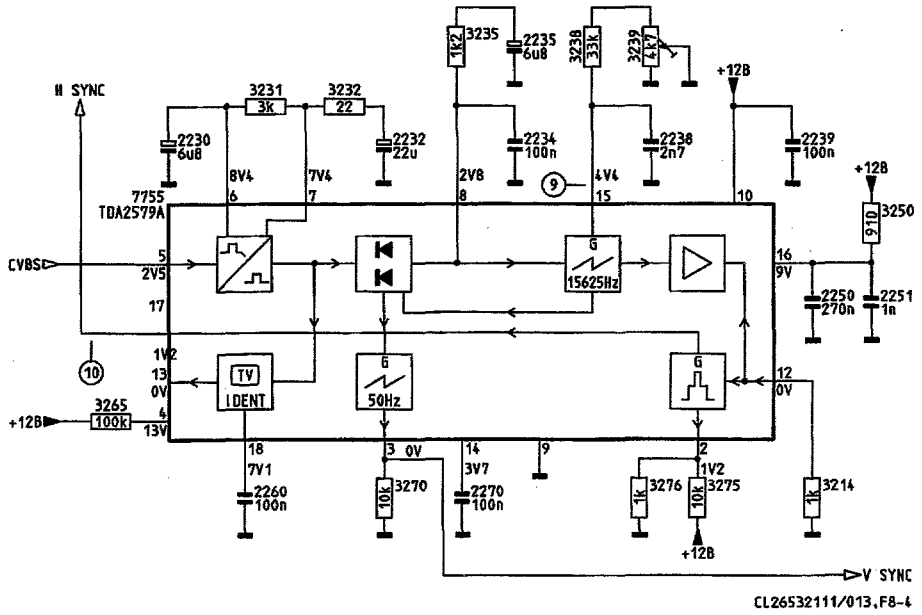


Fig. 8.4

Display synchronisation IC (SDA9086)

The sandcastle of the main picture comes at point 8 of IC7410 via a differential amplifier (see fig. 8.5) and an emitter follower. This IC contains a VCO which shows 27 MHz.
The clock (13.5 MHz) is produced by a PLL circuit which is synchronous with the sandcastle of the main picture and is present at pin 5. (At 50HZ the VCO is divided by 2.)
The horizontal synchronisation pulse (H) is derived from the clock (13.5 MHz/864) and is thus also synchronised with the sandcastle of the main picture.
The PLL compares the divided clock frequency with the signal at point 8 and emits up/down pulses which are smoothed by the RC network at pin 3. Using this the VCO is adjusted until the clock is precisely a multiple of the line frequency of the main picture.

The vertical synchronisation pulse from the field output stage (V_{PIP}) (see section 6.2) is sent to the PIP processor.

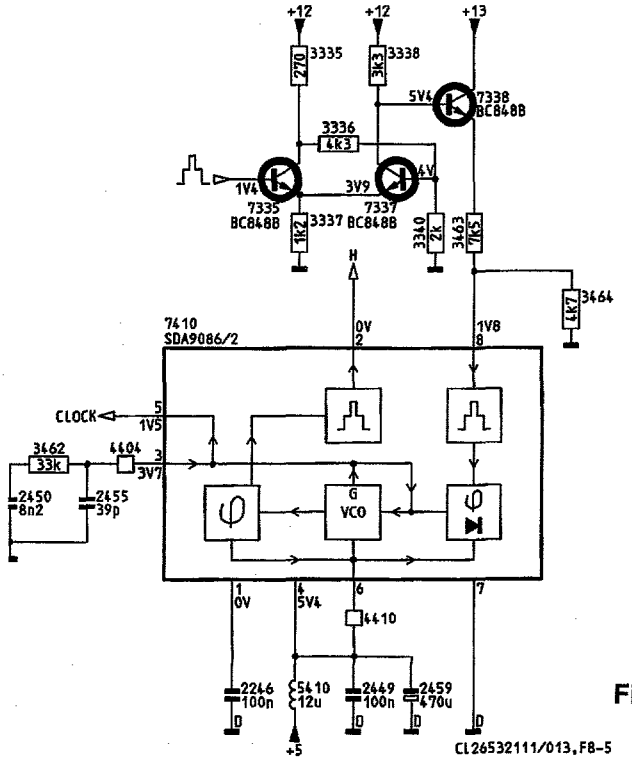


Fig. 8.5

8.5 De A/D converter

Internal clock frequency

The analog-to-digital converter is controlled by an internally produced 13.5 MHz clock frequency (see fig. 8.6). This clock frequency is locked to the clock signal supplied to pin 22 from the display sync IC7410.
The colour difference signals R-Y and B-Y enter the A/D converter via TS7402 and TS7400 via pins 17 and 18, respectively.

The Y signal first goes through a lowpass filter to filter out the chrominance signal and to prevent folding deformation.

Reduced bandwidth

Because the signal still ultimately appears in the PIP picture on the screen with a reduced bandwidth, the filter has a tilting point of only 1.3 MHz.

The reference voltages are determined in IC7406 by voltage dividers between pin 13 (Vref Low) and pin 12 (Vref High).

Colour difference signals multiplexed

Because the bandwidth of the R-Y signal and the B-Y signal is smaller than that of the Y-signal, the sample frequency for R-Y and B-Y may be lower than 13.5 MHz.
Thus, the colour difference signals are multiplexed from 5-bit signals with a sample frequency of 13.5 MHz to 2-bit signals with a sample frequency of 13.5 MHz. This takes place by using only one of each of the 4 samples and dividing the 5 bits of this sample over 2 bits and 4 clock periods (see fig. 8.6).
Because the signals are delayed by this (and by the later demultiplexing), the Y-signal must also be delayed.

Luminance delay

This extra delay takes place by an internal delay line, the delay of which is set by the voltage at pins 20 and 21. With the setting used the delay time is set at 6 clock periods.
A horizontal blanking pulse is obtained from the digital Y-signal, which is passed on to the PIP processor via pin 24, where this pulse is used to synchronise the read-in clock.

Y: 5 bits
R-Y : 2 bits
B-Y : 2 bits

The A.D.C. thus supplies a 5-bit Y-signal, a 2-bits B-Y signal and a 2-bit R-Y signal to the PIP processor.

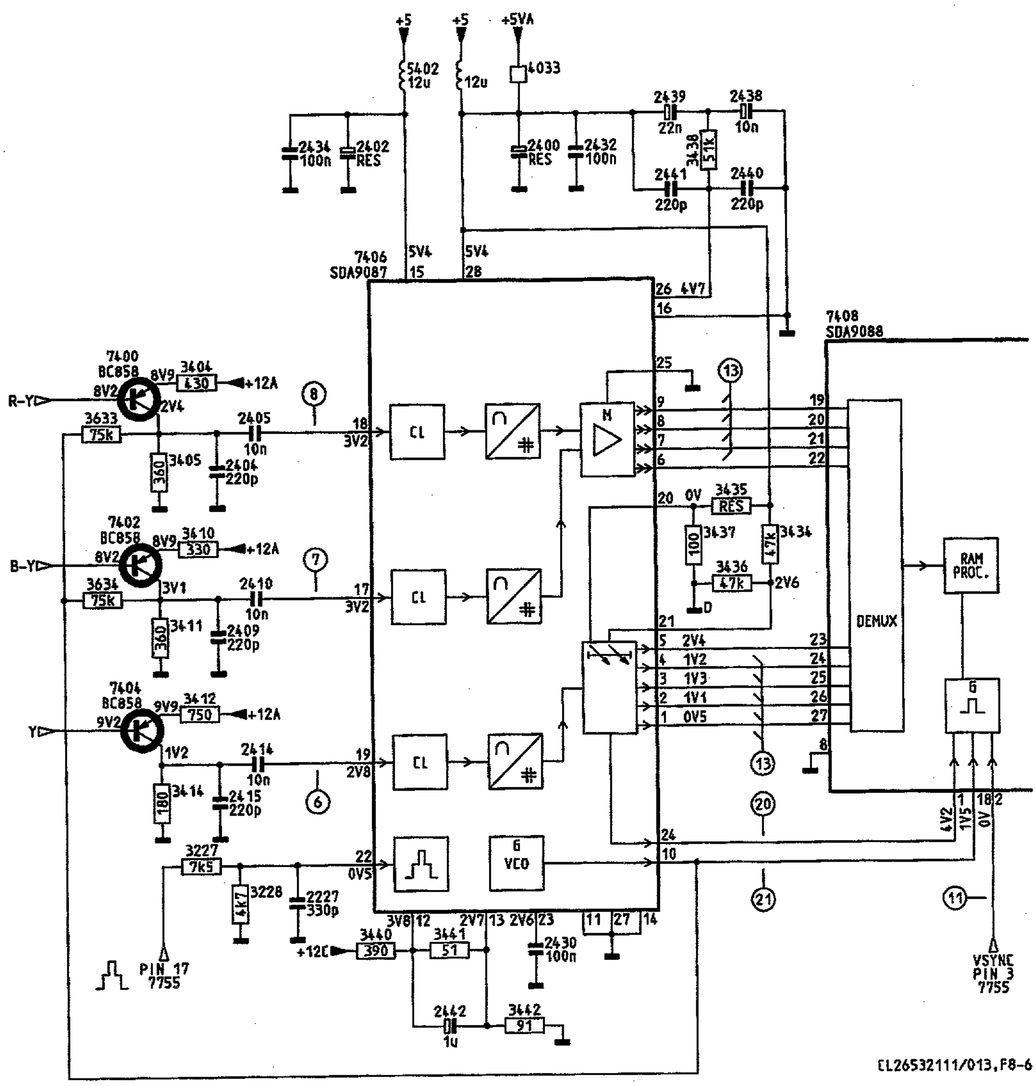

+5
+5
+5VA
5402
12u
12u
4033
2434
100n
2402
RES
2400
RES
2432
100n
2439
22n
2438
10n
3438
51k
2441
220p
2440
220p
7406
SDA9087
5V4
15
5V4
28
26 4V7
16
7408
SDA9088
7400
BC858
8V9
3404
430
+12A
R-Y
8V2
2V4
3633
75k
2405
10n
2406
220p
3405
360
18
3V2
CL
25
9
8
7
6
19
20
21
22
20 0V
3435
RES
3437
100
3434
47k
3436
47k
2V6
D
DEMUX
RAM
PROC.
7402
BC858
8V9
3410
330
+12A
B-Y
8V2
3634
75k
3V1
2410
10n
2409
220p
3411
360
17
3V2
CL
21
5 2V4
4 1V2
3 1V3
2 1V1
1 0V5
23
24
25
26
27
8
7404
BC858
9V9
3412
750
+12A
Y
9V2
1V2
2414
10n
2415
220p
3414
180
19
2V8
CL
3227
7k5
22
0V5
3228
4k7
2227
330p
6
VCO
24
10
3V8 12
2V7 13 2V6 23
11 27 14
3440
390
3441
51
2430
100n
+12C
2442
1u
3442
91
PIN 17
7755
4V2
1V5
0V
1
18 2
VSYNC
PIN 3
7755
CL26532111/013,F8-6

Fig. 8.6

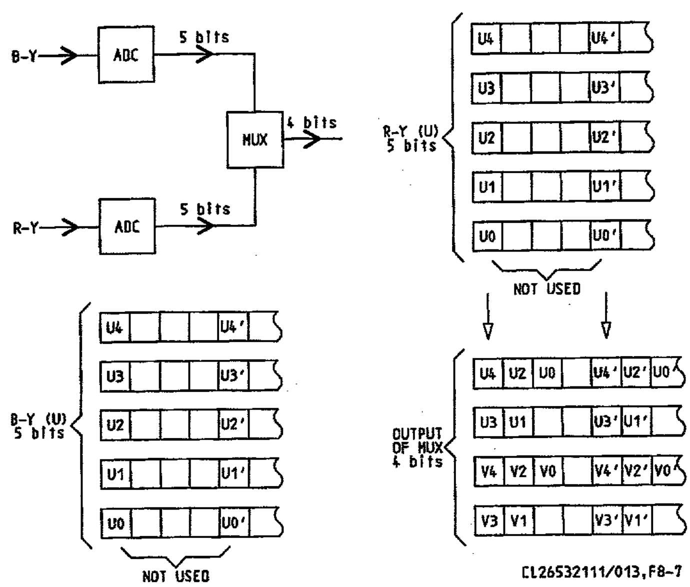
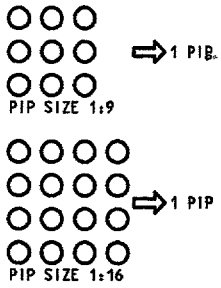

B-Y
ADC
5 bits
MUX
4 bits
R-Y
ADC
5 bits
R-Y (U)
5 bits
U4 U4'
U3 U3'
U2 U2'
U1 U1'
U0 U0'
NOT USED
B-Y (U)
5 bits
U4 U4'
U3 U3'
U2 U2'
U1 U1'
U0 U0'
NOT USED
OUTPUT
OF MUX
4 bits
U4 U2 U0 U4' U2' U0'
U3 U1 U3' U1'
V4 V2 V0 V4' V2' V0'
V3 V1 V3' V1'
CL26532111/013,F8-7

Fig. 8.7



CL26532111/013.F8-8

Fig. 8.8

8.6 The PIP processor

The PIP processor receives one 5-bit Y and two 2-bits (U and V). These colour difference signals are demultiplexed first.

In order to place the PIP picture on a reduced format within the main picture, it must first be compressed. Depending on the PIP size selected, the average of 9 or 16 samples is determined in the decimation filter. This reduction always takes place with 3 or 4 samples in both the horizontal and vertical direction (see fig. 8.7).

In addition to this compression, several lines are left off on the top and bottom of the picture. A number of samples are also left off per line on the left and right. The remaining number of lines and samples is given in table 8.1.

PIP SIZE	NUMBERS OF PIXELS PER LINE			NUMBER OF LINES
1/9	212	53	53	88
1/16	160	40	40	66

Table 8.1

Because the sample frequency for R-Y and B-Y is 4 times lower than for Y, the number of remaining pixels is also 4 times lower.

This reduced information is now stored in the memory using the INSET clock (see section 8.4). The memory is read using the DISPLAY clock (see also section 8.4). In order to convert the read-out Y, R-Y and B-Y signals into a matrix, R, G and B signals must have the same sample frequency. The interpolator fulfils this function.

The interpolator

Three intermediate samples are always calculated and inserted in the interpolator by linear interpolation between two consecutive samples of R-Y and B-Y. Y, R-Y and B-Y now have the same sample frequency (13.5 MHz).

In the PIP frame blanking part a pulse is produced which is high during the presence of the PIP picture. This fast blanking is carried out via pin 9 and is used to blank the main picture when the PIP picture is present.

The RGB matrix

R-Y, B-Y and Y are converted into R, G and B in the matrix.

The DA converter

In the digital-to-analog converter the digital R, G and B signals are converted into analog signals which are then carried out via pins 5, 6 and 7.

EXT RGB / PIP RGB

In IC7380 a selection is made between RGB from EXT1 or RGB PIP using the PIP frame blanking signal.

9. The power supply

Contents

9.1 Introduction

An integrated SOPS (Self Oscillating Power Supply) is employed in the Anubis B. A simple block diagram is shown in Fig. 9.1.

The SOPS is built up around two IC's: a special opto-coupler IC 7514 (CNR50) and the controller IC 7500 (TDA8385).

Some functions on the primary side are:
- control circuit foe the switch transistor (FET)
- start circuit
- undervoltage protection

Some functions on the secondary side are:
- voltage regulation
- stand-by function
- excess voltage protection

The switching period of the switching transistor (FET) TS7525 can be divided into two main areas (see Fig. 9.2):
T_{on}: switch-FET is conducting; energy is stored in the transformer.
T_{off}: switch-FET blocks; energy in the transformer is transferred to the secondary side.
T_{off-n}: switch-FET blocks; once all energy is transferred the primary coil of the transformer oscillates with C2524 (capacitor over the FET).
The FET T_{on} is adjustable and is dependent on the load and the input voltage (280V DC) of the SOPS. To keep the switching losses as low as possible the FET is switched in at the moment that the drain source voltage U_{ds} is at its minimum.

The opto-coupler IC 7514 (CNR50) controls the FET switching. The opto-coupler LED is controlled by control IC 7500 (TDA8385).

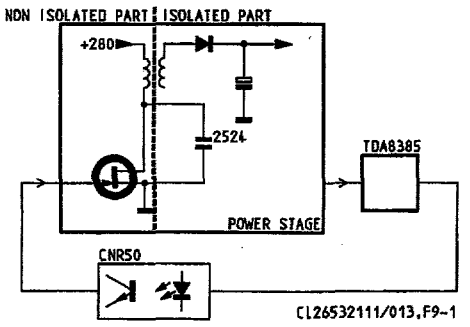


Fig. 9.1

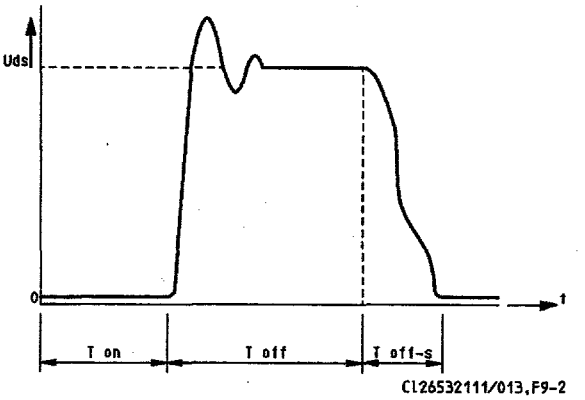


Fig. 9.2

9.2 The primary side

Power supply and initialisation of the CNR50 (Fig. 9.3)

The CNR50 is fed from C2511 which is loaded via resistors R3514 and 3515 from the rectified mains voltage. If the voltage over capacitor C2511 (power supply voltage from the CNR50) is greater than 14.8V and the voltage over R3529 is greater than 2.95V the CNR50 will start up.
Once the CNR50 has started the output on pin 6 will supply a 1 mA current to the gate of the switching FET. At the moment that the Vgs threshold of the FET is reached it will begin conducting. Winding 6-8 will now take over the opto-coupler power supply before C2511 has discharged to below 3.9V (the minimum power supply voltage of the CNR50).

Undervoltage protection

The level of the SOPS input voltage (280V DC) is detected by pin 7 of the CNR50 via the voltage divider 3529/3518. If the voltage is greater than 2.9V (250 DC input voltage) then start up is possible. If the voltage drops below 2.35V (200V DC input voltage) the power supply will cease (undervoltage protection). This ensures that the control IC (TDA8385) and the switching FET do not operate with a power supply that is too low.

SOPS start up

If the CNR50 has started and the switching FET is conducting, the control voltage V_{gs} is taken over by winding 9-6 (forward winding in comparison to winding 1-7) and the FET is taken further into and held in conduction.
If IC 7500 (TDA8385) has started the LED on the CNR50 is switched in. The output of the CNR50 (pin 6) becomes 0.5V and the switching FET is switched out.
If the FET is switched out the energy in the transformer is transferred to the secondary side. At the moment the energy transfer is complete the polarity of all voltages in the transformer reverse. This is detected by IC7500 (TDA8385) with as a result: LED off, FET on, energy storage in transformer, LED on, FET off, energy transfer, LED off, FET on, etc.

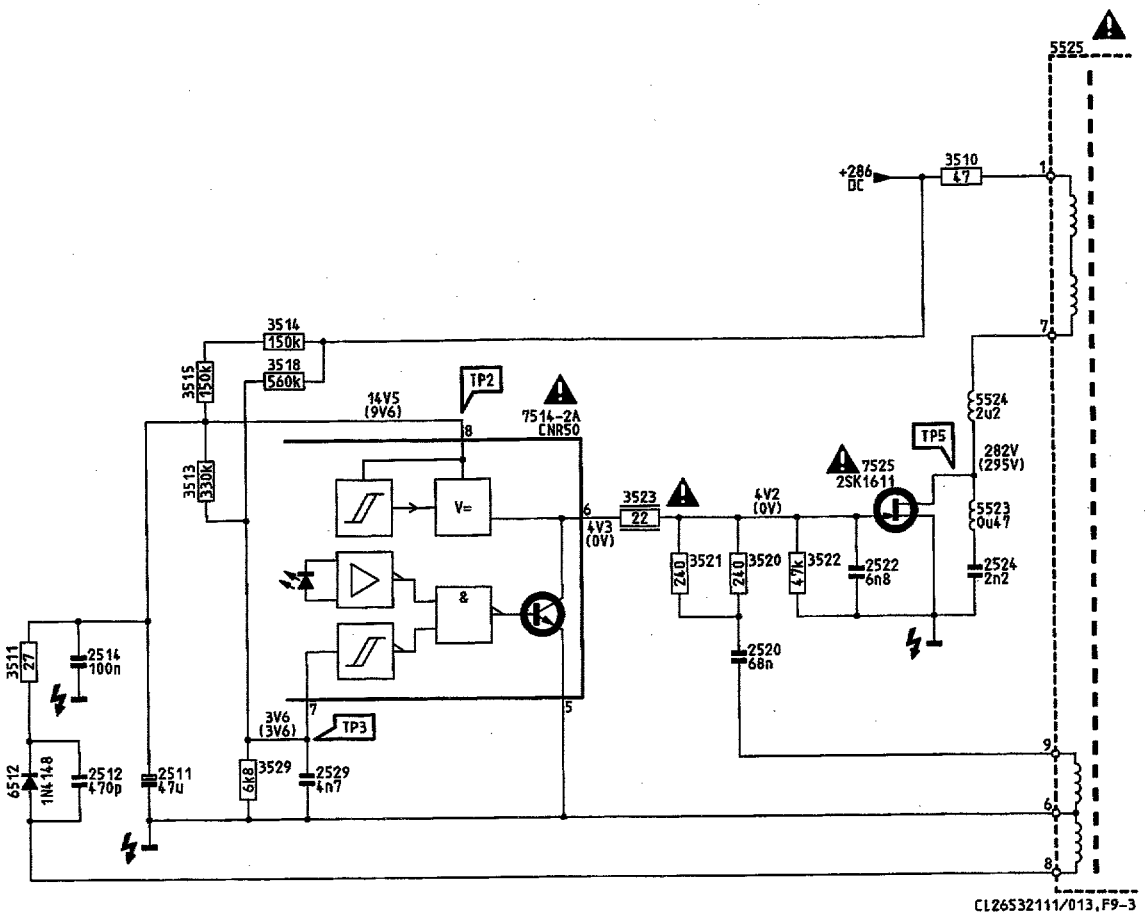


Fig. 9.3

9.3 The secondary side

The TDA8385

The TDA8385 is fed from winding 16-10 (see Fig. 9.4). The power supply voltage on pin 16 of IC 7500 has to lie between 7.5V and 20V. The IC will not operate until the power supply voltage has reached 7.5V (the LED in the opto-coupler will not be operated). Subsequently the power supply voltage on pin 16 may drop to 5.2V. The power supply voltage has to be rapidly available to ensure the good operation of the IC, therefore C2547 is an electrolytic capacitor with an extremely low internal resistance (special type).

The sawtooth generator

The drain-source current I_{ds} of the switching FET is indirectly detected via winding 16-10 and R3547 on pin 12 of the TDA8385 (C2562). If the switching FET is switched out C2562 discharges via an internal switch resulting in a sawtooth voltage over C2562. The level of the sawtooth voltage is therefore a measure of the voltage through the switching FET.

The pulse width modulator

The output voltage of the power supply circuit (+97.5V power supply) is coupled back to pin 9 via resistors R3531, R3534 and R3535 and compared with the sawtooth voltage from the sawtooth generator. At the moment that the sawtooth voltage becomes higher than the measured voltage the output of the pulse width modulator goes high and the LED is switched in. The switching FET is switched out.

Slow start mechanism

The slow start mechanism improves the operational reliability of the power supply circuit during start up. During the start up of the power supply circuit, capacitor C2564 is slowly charged. The voltage level of this capacitor is converted in the TDA8385 to a $T_{on\text{-}max}$ for the switching FET, and therefore determines the maximum current I_{xx} which can travel through the switching FET. In this manner the $T_{on\text{-}max}$ can be slowly built up during start up.
This slow start mechanism is activated when switching the set on, when starting up from stand-by and during any overload or short circuiting.

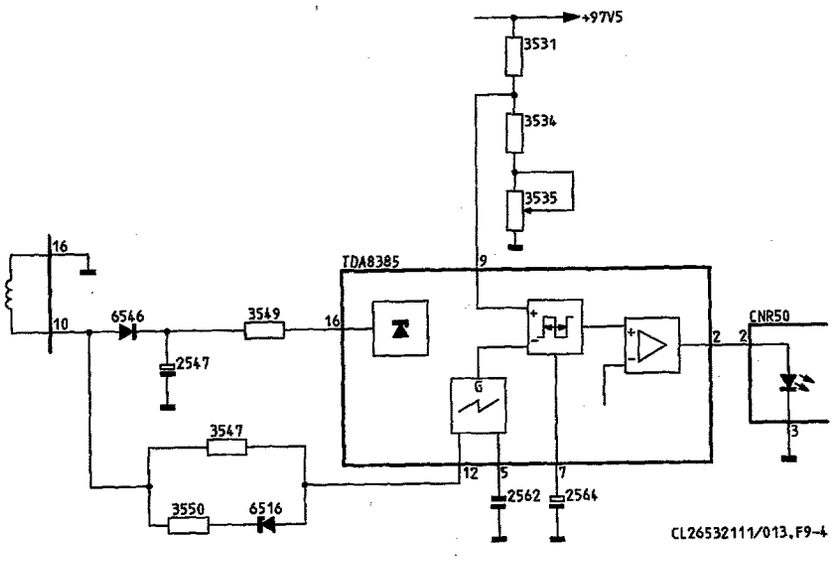


Fig. 9.4

Stand-by (Fig. 9.5)

In stand-by the power supply operates following the burst mode principle (power supply on for a short time, then off for a short time).
Unlike the GR2 power supply, the Anubis B has no stand-by thyristor. The output voltages in stand-by drop very little incomparison to the nominal voltage values (70-90%). For this reason a special circuit (R3388, R3383, D6385, C2386, R3382, TS7388, R3381, R3382 and D6384) causes the line output stage to be switched out during stand-by, and started slowly when starting up from stand-by.

During stand-by transistor 7573 does not conduct (stand-by signal of the µP is active low). This causes the voltage on pin 10 of TDA8385 to become greater than 2.5V which takes TDA8385 into the stand-by mode. The TDA8385 stand-by mode is arranged in hysteresis:
Once the voltage on pin 10 of the TDA8385 (the voltage over C2560 divided by 3569/3571 that therefore forms a reflection of the output voltages of the SOPS during stand-by) is greater than 2.5V, the FET switches out.
Once the voltage on pin 10 of the TDA8385 drops below 2.0V the so-called burst is activated. (FET switches in/out with a maximum frequency; a maximum frequency because the non-conducting transistor TS7573 causes transistor TS7572 to conduct and short C2564, through which T_{on} is always at minimum during stand-by mode).

Protection (Fig. 9.6)

Excess voltage situations are reported on pin 8 of the TDA8385. If the voltage on pin 8 is greater than 2.5V then the CNR50 LED conducts continuously so that the FET does not conduct.
The power supply to the TDA8385 is cut off, the LED extinguishes and the power supply starts up again. If excess voltage is still present the procedure will repeat (hic-mode).

9.4 Protected circuits (fig 9.6)

Excess voltage protection (SOPS)

The power supply circuit is protected from excess voltage by zener diode D6565. If the voltage on C2560 (unstabilised +5V) is higher than +15V the protection is activated and the power supply circuit switched out.

High voltage protection (LOT)

If the level of the line flyback pulse increases (and therefore the high voltage too), due to a fault in the line circuit for example, the voltage on pin 10 of the LOT will also be higher. If this voltage becomes too high D6469 and zener diode D6564 will conduct and the power supply circuit protection activated.

Beam current protection (BCI)

In principle the beam current travels through R3460 and R3461 and is translated into a voltage (Beam Current Info) over these resistors. If the voltage over these resistors increases (increased beam current) the power supply circuit protection will be activated via R3472, R3478, R3480, R3474, D6472, R3467 and D6564.

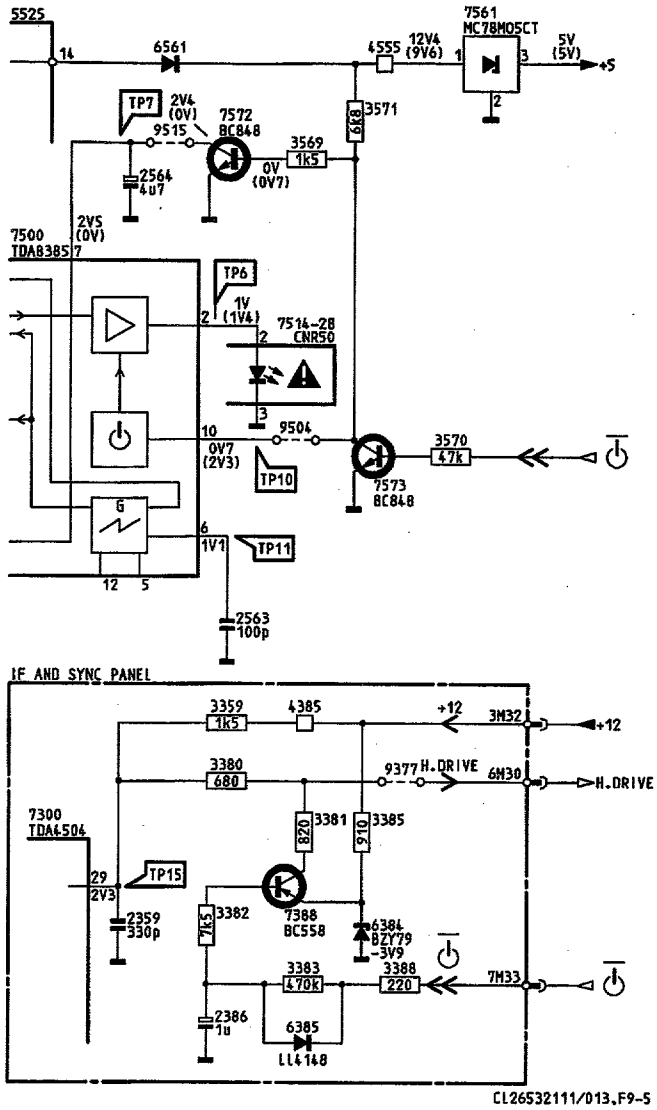

5525
14
6561
7561
MC78M05CT
4555
12V4
(9V6)
5V
(5V)
+5
TP7
2V4
(0V)
9515
7572
BC848
3571
6K8
3569
1K5
0V
(0V7)
2564
4u7
2V5
(0V)
7500
TDA8385
7
TP6
1V
(1V4)
7514-28
CNR50
9504
10
0V7
(2V3)
TP10
3570
47k
7573
BC848
G
6
1V1
TP11
12
5
2563
100p
IF AND SYNC PANEL
3359
1k5
4385
+12
3M32
+12
3380
680
9377 H.DRIVE
6M30
H.DRIVE
7300
TDA4504
820
3381
910
3385
29
2V3
TP15
2359
330p
7k5
3382
7388
BC558
6384
BZY79
-3V9
3383
470k
3388
220
7M33
2386
1u
6385
LL4148
CL26532111/013.F9-5

Fig. 9.5

Overscan protection

A fault condition can lead to a horizontal deflection which is too great and a beam current on the sides of the picture tube. This can result in overscan. To avoid this any E/W voltage which is too high is measured via 6476 and 6564 and the power supply circuit protection activated.

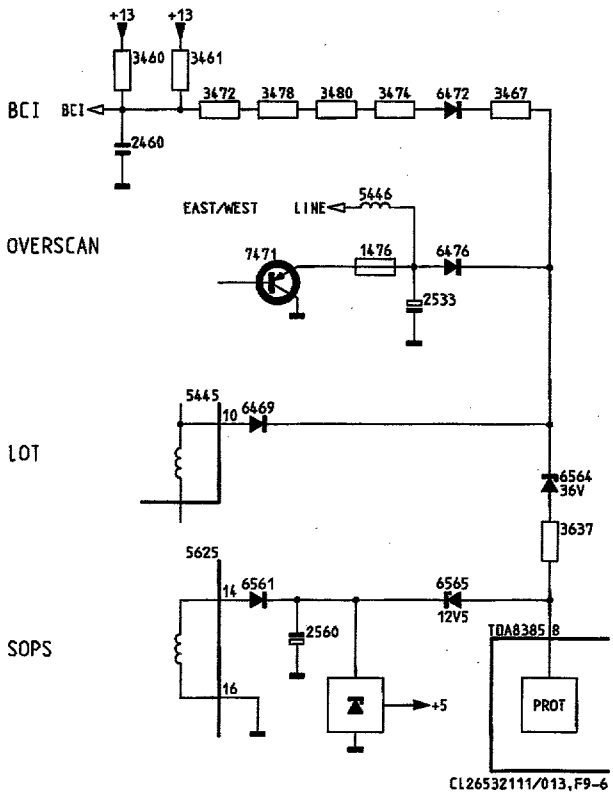


Fig. 9.6

9.5 Service tips

C2547 is a special type with a very low impedance. It may therefore only be replaced with the prescribed type.